CMPE 691: Digital Signal Processing Hardware Implementation

Course Master

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Other Faculty N/A

Lecture

MW 4:00-5:15 pm
ITE 375

Office hours

After lecture or by appointment

Webpage

http://www.csee.umbc.edu/~tinoosh/cmpe691/

Check frequently for class news, handouts, papers, and assignments.

Prerequisites

CMPE 310, CMPE 415

Grading: Letter

50% Homework/minor projects
20% Midterm Exam
20% Final project and presentation
5% Quizzes
5% Classroom participation

Proposed Catalog Course Description

This graduate course will investigate implementations of digital signal processing and communication algorithms in hardware (including FPGAs and ASICs) and will investigate the use of DSP hardware in modern applications such as mobile phones, biomedical devices and satellite transceivers. Emphasis is on digital signal processors, design implementation on FPGA/ASIC fabrics and test real systems on board, architectures, control, functional units, and circuit topologies for increased performance and reduced circuit size and power dissipation.

General Course Description & Objectives

Through this course, students will develop the necessary skills to design simple processors suitable for numerically intensive processing with an emphasis on FPGA/ASIC implementation flow.

Specifically, the course will investigate:

1) High-level DSP optimizations such as pipelining, unfolding, and parallel processing

2) Common DSP and communication algorithms such as FFTs, finite impulse response (FIR) filters, direct digital frequency synthesizers, correlators and error correction.

3) Modeling of DSP algorithms in Matlab and conversion of Matlab models into fixed-point Verilog blocks

4) System implementation on FPGA boards and verification

5) Platform implementation issues: hardware vs. software, FPGA vs. ASIC, power, area, throughput, etc.

6) Applications of DSP hardware such as mobile phones, biomedical devices, satellite receivers and software defined radios

Topical Outline

I. Digital signal processing overview
- A. DSP workloads
- B. Example applications

II. Processor building blocks
- A. Quick review of Verilog hardware description language
- B. Binary number representations
- C. Types of Adders and Multipliers
- F. Fixed-input multipliers (optimizations)
- G. Complex arithmetic hardware
- H. Memories

III. DSP and Communication algorithms and systems
- A. LDPC Decoding
- B. FIR filtering
- C. Multi-rate signal processing
- B. Processor control and datapath integration
- D. Example systems: FFT, LDPC Decoder/Encoder, OFDM, biomedical imaging

IV. Design optimization
- A. Platform implementation fabrics FPGAs and ASICs
- B. Verilog synthesis to a gate netlist
- C. Delay estimation and reduction
- D. Area estimation and reduction
- E. Power estimation and reduction

Course weekly Schedule

Week	Handout/Reading (Slides are available in website)	Topics	HW or Readings
1	Chapter 3, Peter J. Ashenden 1:SignExtension	Course introduction, DSP overview, MAC; FIR, convolution, dot products; Number representations, sign extension, Redundant representations; Adders: carry-propagate vs. carry-save, subtraction, ripple, carry-select adders	Programmable DSP Architectures: Part I Edward A. Lee
2	Chapter 3, Peter J. Ashenden 2:EfficMultInputAddition, 4:ExampMult, 5:Verilog	Carry-lookahead adders; multiple-input sign extension, multipliers, verilog	Quick Reference For Verilog, Rajeev Madhavan HW1: Binary arithmetic, verilog, and many-input adders
3	5:FPGA flow	FPGA Design Flow	
4	6:Error Correction	Communications Systems, Modulations, error correction	
5	7:LDPC	Low Density Parity Check (LDPC) decoding LDPC decoder hardware implementation Area, speed, power tradeoffs	HW2: Synthesis and Place and route, LDPC decoder
6	Chapter 4, Peter J. Ashenden 7:VerilogTesting, 8:VerilogControl,	control circuits, state machine design, Squaring, fixed-input multiplies Complex arithmetic, complex rotations, conversions, and amplitude estimation, Saturation, rounding	
7	9:dB, 17:FiltCoeffDesign, 10:SignalMags 11:FilterResponse, 12:FIRScaling,	Fourier Transform II, DFT, filters, filter design	

8	13:DFT&FFTbackground, 14:FFTdiagrams 15:FFTalgs	The Fast Fourier Transform, Implementing FFT processors	HW3: Filters, FFT
9		Midterm	
10	16: Seizure detection	Seizure detection Seizure detection hardware	
11	17:Multi-rate, 18:Upsampling, 19:Decimation, 20:DCoffset	Convolution using DFT/FFTs, Upsampling, decimation, DC offset, Automatic gain control	
12	21:Imaging hardware	Biomedical imaging, Ultrasound Imaging	Final Project: seizure detection and transmission
13		Ultrasound imaging hardware implementation	
14	Chapter 4, Peter J. Ashenden 22: Implementation fabrics	FPGA vs ASIC implementation	
15		Final project presentation	

Texbook

Digital Design an Embedded Systems Approach Using VERILOG, Peter J. Ashenden, ISBN: 978-0-12-369527-7, Morgan Kaufmann, 2008.

VLSI Digital Signal Processing Systems: Design and Implementation, Keshab K. Parhi, ISBN: 978-0471241867, Wiley, 1999.

Suggested references

The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, ISBN: 0750676043

Digital Signal Processing with Field Programmable Gate Arrays, Uwe Meyer-Baese, 3rd Edition, Springer, 2007, ISBN: 978-3540726128.

Verilog According to Tom (available on course web page), Tom Chanak

Quick Reference for Verilog HDL (available on course web page), Rajeev Madhavan

Digital Signal Processing: Principles, Algorithms, and Applications, John G. Proakis and Dimitris K. Manolakis, 4th edition, Prentice Hall, 2006, ISBN: 978-0131873742. [3rd edition also fine]

Discrete-Time Signal Processing, Alan V. Oppenheim, Ronald W. Schafer, and John R. Buck, 2nd edition, Prentice Hall, 1999, ISBN: 978-0137549207.

Disabilities

Students who are covered under the American Disabilities Act should inform the teacher privately of this fact so that appropriate instructional arrangements can be made.

Academic integrity

Cheating in this course will cause you to fail the course. You are encouraged to consult the instructor if you have any questions on homework, projects and/ or exams. By enrolling in this course, each student assumes the responsibilities of an active participant in UMBC's scholarly community in which everyone's academic work and behavior are held to the highest standards of honesty. Cheating, fabrication, plagiarism, and helping others to commit these acts are all forms of academic dishonesty, and they are wrong. Academic misconduct could result in disciplinary action that may include, but is not limited to, suspension or dismissal. Consult the UMBC Student Handbook to read the full Student Academic Conduct Policy.

Late work policy

If assignment is reviewed in class, no credit is possible for late work. If assignment was not reviewed in class, there will be a 1/3 reduction of remaining credit per day (i.e., 100% -> 67%, 44% -> 30% ...).

Regrading policy

Please bring clear grading errors to my attention. Non-obvious grading issues will not be considered due to fairness to all students, and the inherent subjectiveness of grading.

References list

1. B. M. Baas, An Approach to Low-power, High-performance, Fast Fourier Transform Processor Design, Ph.D. thesis, Stanford University, Stanford, CA, USA, 1999
2. Zhengya Zhang, Design of LDPC Decoders for Improved Low Error Rate Performance, Ph.D thesis, University of California Berkeley, CA, USA, 2009
3. Digital Design an Embedded Systems Approach Using VERILOG, Peter J. Ashenden, ISBN: 978-0-12-369527-7, Morgan Kaufmann, 2008.
4. VLSI Digital Signal Processing Systems: Design and Implementation, Keshab K. Parhi, ISBN: 978-0471241867, Wiley, 1999.
5. The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, ISBN: 0750676043
   Digital Signal Processing with Field Programmable Gate Arrays, Uwe Meyer-Baese, 3rd Edition, Springer, 2007, ISBN: 978-3540726128.

6. Verilog According to Tom, Tom Chanak
7. Quick Reference for Verilog HDL, Rajeev Madhavan
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9. Discrete-Time Signal Processing, Alan V. Oppenheim, Ronald W. Schafer, and John R. Buck, 2nd edition, Prentice Hall, 1999, ISBN: 978-0137549207.