# Power Estimation

# Welcome

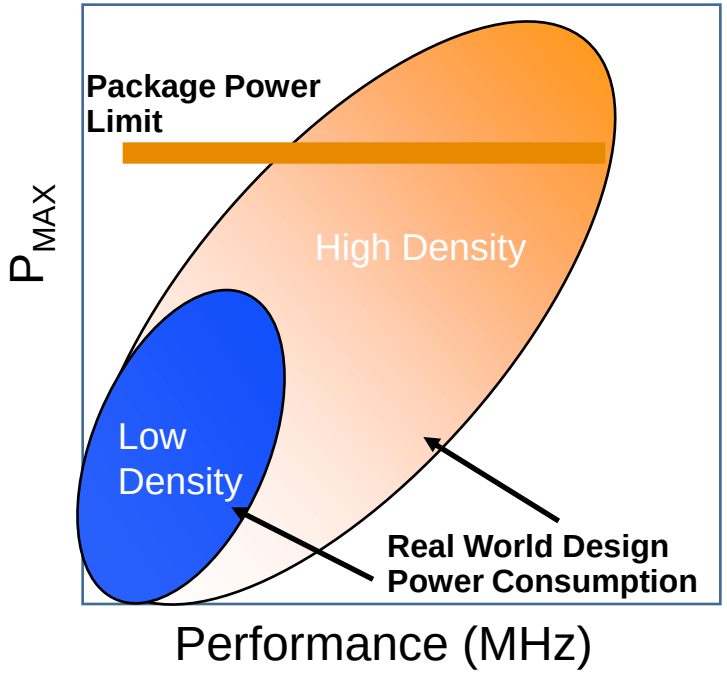
- If you are new to FPGA design, this module will help you estimate your FPGA power consumption
- These design techniques promote fast and efficient FPGA design development

## After completing this module, you will able to:

- List the three phases of the design cycle where power calculations can be performed
- Estimate power consumption by using the XPower Estimator spreadsheet
- Estimate power consumption by using the XPower software utility

# Power Consumption Overview

- As devices get larger and faster, power consumption goes up
- First-generation FPGAs had
  - Lower performance
  - Lower power requirements
  - No package power concerns
- Today's FPGAs have
  - Much higher performance
  - Higher power requirements
  - Package power limit concerns
  - A System Monitor that provides active monitoring of the die temperature
    - Refer to the Virtex-6 User Guide for more information



# Power Consumption Concerns

- High-speed and high-density designs require more power, leading to higher junction temperatures
- Package thermal limits exist
  - 125° C for plastic
  - 150° C for ceramic
- Power directly limits
  - System performance
  - Design density
  - Package options
  - Device reliability

# Estimating Power Consumption

- Estimating power consumption is a complex calculation
  - Power consumption of an FPGA is almost exclusively dynamic
  - Power consumption is dependent on design and is affected by
    - Output loading
    - System performance (switching frequency)
    - Design density (number of interconnects)
    - Design activity (percent of interconnects switching)
    - Logic block and interconnect structure
    - Supply voltage

# Estimating Power Consumption

- Power calculations can be performed at three distinct phases of the design cycle
  - Concept phase: A rough estimate of power can be calculated based on estimates of logic capacity and activity rates
    - Use the Xilinx Power Estimator spreadsheet
  - Design phase: Power can be calculated more accurately based on detailed information about how the design is implemented in the FPGA
    - Use the XPower Analyzer
  - System Integration phase: Power is calculated in a lab environment
    - Use actual instrumentation
- Accurate power calculation at an early stage in the design cycle will result in fewer problems later

# Activity Rates

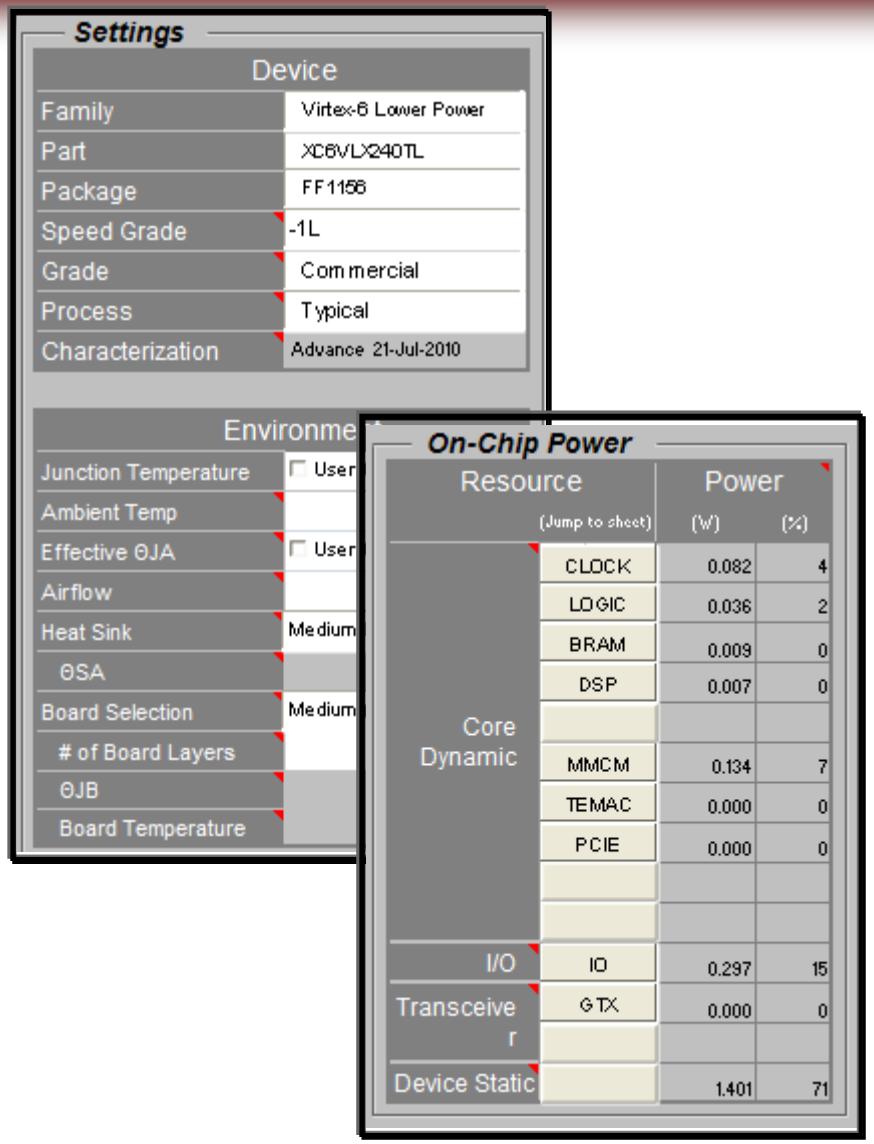
- Accurate activity rates (also known as toggle rates) are required for meaningful power calculations
- Clocks and input signals have an absolute frequency
- Synchronous logic nets use a percentage activity rate
  - 100% indicates that a net is expected to change state on every clock cycle
  - Allows you to adjust the primary clock frequency and see the effect on power consumption
  - Can be set globally to an average activity rate on groups or individual nets
- Logic elements also use a percentage activity rate
  - Based on the activity rate of output signals of the logic element
  - Logic elements have capacitance

# Xilinx Power Estimator

- Excel spreadsheets with power estimation formulas built in
  - Enter design data in white boxes
  - Power estimates are shown in gray boxes
- Sheets
  - Summary (device totals)
  - Clock, Logic, I/O, Block RAMs, DSP, MMCM
  - GTX, TEMAC, PCIE
- To download go to http://www.support.xilinx.com -> *Technology Solutions* -> *Power*
  - Download the XPE spreadsheet for your device family
    - XPE is not installed with the ISE software
  - The Power Solutions page has numerous resources

# Xilinx Power Estimator

- Summary and Quiescent power
  - White boxes allow you to enter design data
  - Gray boxes show you the Power estimates
  - Tabs at bottom allow you to enter power information per device resources (not shown)
  - Settings reviews device, system, and environment information
  - On-Chip Power breaks the estimated power consumption into device resources



# Xilinx Power Estimator

- Summary and Quiescent power
  - Power Supply reviews what power sources will be necessary
  - Summary describes your systems total power and estimated junction temperature

**Power Supply**

| Source | Voltage (V) | Total All |
|---|---|---|
| $V_{CCINT}$ | 0.900 | 1.304 |
| $V_{CCAUX}$ | 2.500 | 0.195 |
| - | | |
| $V_{CCO}$ 2.5 | 2.500 | 0.112 |
| $V_{CCO}$ 1.8 | 1.800 | 0.000 |
| $V_{CCO}$ 1.5 | 1.500 | 0.000 |
| $V_{CCO}$ 1.2 | 1.200 | 0.000 |
| $MGTAV_{CC}$ | 1.000 | 0.000 |
| $MGTAV_{TT}$ | 1.200 | 0.000 |
| - | | |
| - | | |
| - | | |
| - | | |
| - | | |

**Summary**

| | | |
|---|---|---|
| Junction Temperature | 52.9 °C | |
| Total On-Chip Power | 1.967 W | |
| Thermal Margin | 32.1°C | 21.4W |
| Effective θJA | | 1.5 °C/W |

| | | |
|---|---|---|
| 0% | Transceiver..... | 0.000W |
| 15% | I/O..... | 0.297W |
| 14% | Core Dynamic.. | 0.269W |
| 71% | Device Static..... | 1.401W |
| | Power supplied to off-chip devices.. | 0.000W |

# Xilinx Power Estimator

- Clock power

| Name | Frequency (MHz) | Type | Fanout | Clock Buffer Enable | Slice Clock Enable | Power (W) |
|---|---|---|---|---|---|---|
| clock_a | 100.0 | Global | 1000 | 100% | 50% | **0.010** |
| clock_b | 200.0 | Global | 1000 | 100% | 50% | **0.020** |
| clock_c | 250.0 | Global | 4000 | 100% | 50% | **0.053** |
| | 0.0 | Global | 0 | 100% | 50% | 0.000 |

- Logic power

| Name | Clock (MHz) | LUTs as | | | FFs | Toggle Rate | Average Fanout | Power (W) |
|---|---|---|---|---|---|---|---|---|
| | | Logic | Shift Registers | Distributed RAMs | | | | |
| ctrl_block | 200.0 | 2000 | 100 | 100 | 2000 | 12.5% | 3.00 | **0.023** |
| messenger_block | 100.0 | 1000 | 0 | 0 | 1000 | 12.5% | 3.00 | **0.005** |
| state_machine | 250.0 | 150 | 0 | 0 | 1250 | 12.5% | 3.00 | **0.008** |

| Name | I/O Settings | | | | | | | Activity | | | | Output Load (pF) | On Chip Power (W) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | I/O Standard | Input Pins | Output Pins | Bidir Pins | IO LOGIC SERDES | IO DELAY | IBUF LOW PWR | Clock (MHz) | Toggle Rate | Data Rate | Output Enable | | $V_{CCINT}$ 0.9V | $V_{CCAUX}$ 2.5V | $V_{CCO}$ all rails |
| control_outputs | LVCMOS 2.5V 12mA (Slow) | 0 | 80 | 0 | No | Off | Yes | 100.0 | 12.5% | SDR | 100.0% | 0 | **0.001** | **0.004** | **0.062** |
| processor_outputs | LVCMOS 2.5V 12mA (Slow) | 0 | 50 | 0 | No | Off | Yes | 150.0 | 12.5% | SDR | 100.0% | 0 | **0.001** | **0.004** | **0.058** |
| communicator | LVCMOS 2.5V 12mA (Slow) | 0 | 100 | 0 | No | Off | Yes | 200.0 | 12.5% | SDR | 100.0% | 0 | **0.002** | **0.011** | **0.155** |

- I/O power

# Xilinx Power Estimator

- Block RAM, DSP, and MMCM power

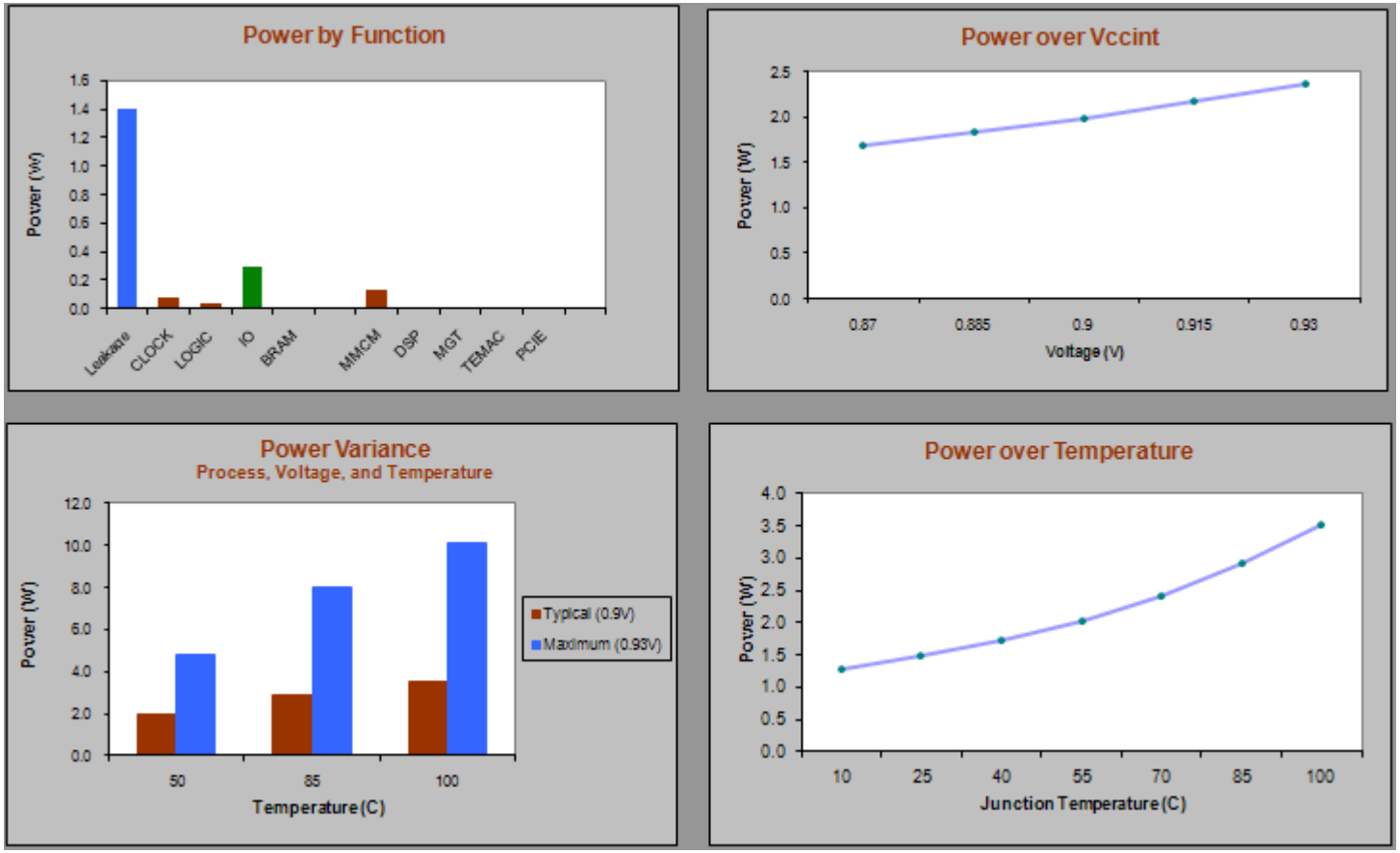
| Name | BRAMs | Mode | Toggle Rate | Clock (MHz) | Enable Rate | Bit Width | Write Mode | Write Rate | Clock (MHz) | Enable Rate | Bit Width | Write Mode | Write Rate | Power (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| memory_bank_a | 6 | RAMB18 | 50.0% | 100.0 | 25.0% | 1 | WRITE_FIRST | 50.0% | 0.0 | 25.0% | 1 | WRITE_FIRST | 50.0% | **0.001** |
| memory_bank_b | 10 | RAMB18 | 50.0% | 150.0 | 25.0% | 1 | WRITE_FIRST | 50.0% | 0.0 | 25.0% | 1 | WRITE_FIRST | 50.0% | **0.003** |
| memory_bank_c | 10 | RAMB18 | 50.0% | 200.0 | 25.0% | 1 | WRITE_FIRST | 50.0% | 0.0 | 25.0% | 1 | WRITE_FIRST | 50.0% | **0.004** |

| Name | DSP Slices | Clock (MHz) | Toggle Rate | MREG Used? | MULT Used? | Pre-add Used? | Power (W) |
|---|---|---|---|---|---|---|---|
| Filter | 4 | 250.0 | 12.5% | Yes | Yes | No | **0.003** |
| Transform | 4 | 200.0 | 12.5% | Yes | Yes | No | **0.002** |
| Multiplier | 6 | 100.0 | 12.5% | Yes | Yes | No | **0.002** |

| Name | Clock (MHz) | Phase Shift | Divide Counter | Multiply Counter | Clock 0 Divide | Clock 1 Divide | Clock 2 Divide | Clock 3 Divide | Clock 4 Divide | Clock 5 Divide | Clock 6 Divide | $V_{CCINT}$ (W) | $V_{CCAUX}$ (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| clock_a | 100.0 | None | 1 | 2 | off | off | off | off | off | off | off | **0.001** | **0.044** |
| clock_b | 150.0 | None | 1 | 1 | off | off | off | off | off | off | off | **0.001** | **0.042** |
| clock_c | 200.0 | None | 1 | 1 | off | off | off | off | off | off | off | **0.001** | **0.045** |

# Xilinx Power Estimator

- Graphs

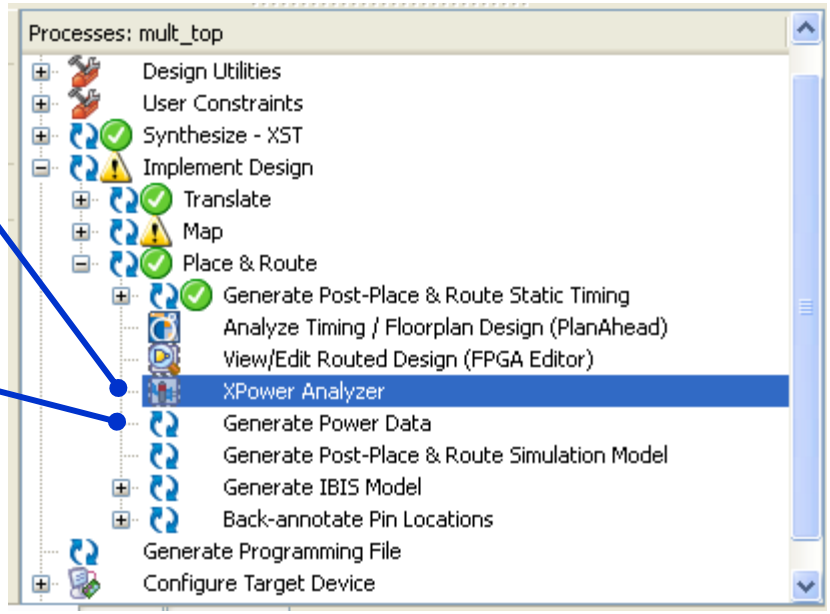


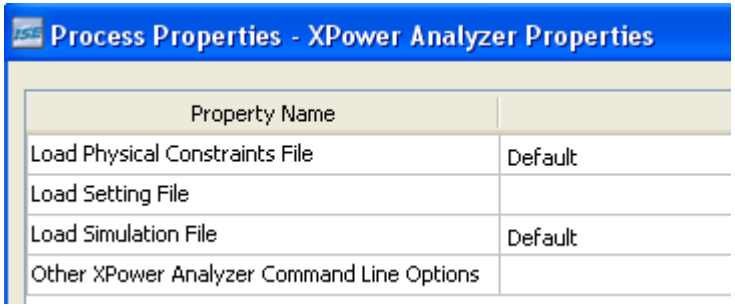
# What is the XPower Analyzer?

- A utility for estimating the power consumption and junction temperature of FPGA and CPLD devices
- Reads an implemented design (NCD file) and timing constraint data
- You supply activity rates
  - Clock frequencies
  - Activity rates for nets, logic elements, and output pins
  - Capacitive loading on output pins
  - Power supply data and ambient temperature
  - Detailed design activity data from simulation (VCD file)
- The XPower Analyzer calculates the total average power consumption and generates a report

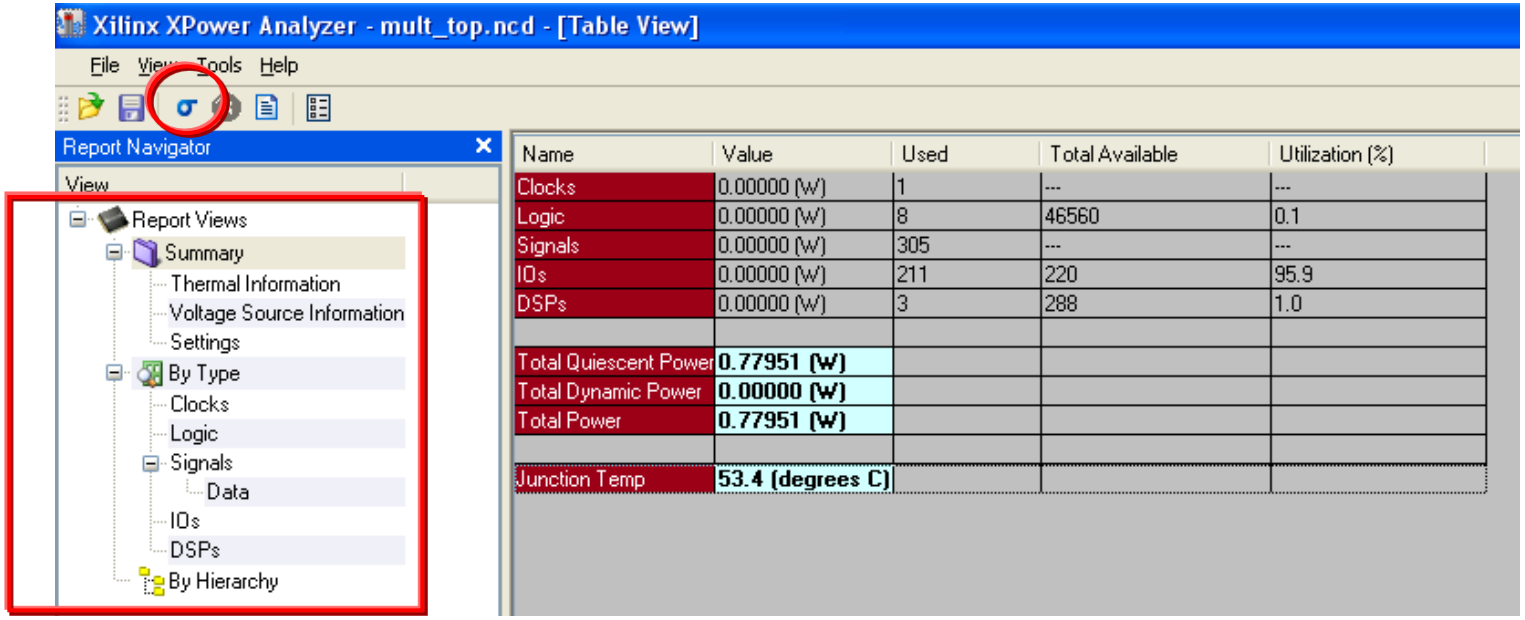
# Running the XPower Analyzer

- Expand **Implement Design → Place & Route**
- Double-click **XPower Analyzer** to launch the XPower utility in interactive mode
- Use the **Generate Power Data** process to create reports using VCD files or TCL scripts



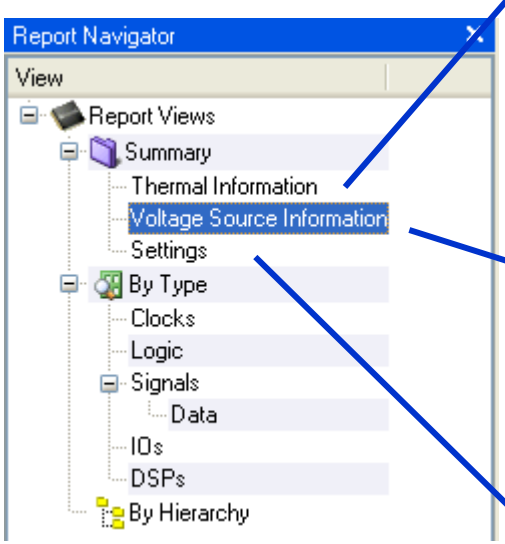



# Summary




- Estimated junction temperature
- Reporting, settings, and thermal information is all placed in one utility
  - As you manipulate system characteristics you will update the generated report
- Report Navigator allows for quick migration to various reports and functions of the utility

# Report Navigator




| Name | Value | Range |
|---|---|---|
| Ambient Temp (degrees C) | 60.0 | 0.0 to 85.0 |
| User Junction Temp (degrees C) | | |
| Use custom ThetaJA ? | No | |
| Custom ThetaJA (degrees C/W) | NA | |
| Airflow (LFM) | 250 | |
| Heat Sink | None | |
| Custom ThetaSA (degrees C/W) | NA | |
| Board Selection | Medium (10"x10") | |
| # of Board Layers | 8 to 11 | |
| Custom ThetaJB (degrees C/W) | NA | |
| Board Temperature (degrees C) | NA | |
| | | |
| Effective ThetaJA (degrees C/W) | 6.5 | |
| Max Ambient (degrees C) | 77.8 | |
| Junction Temp (degrees C) | 67.2 | |

- Thermal Information

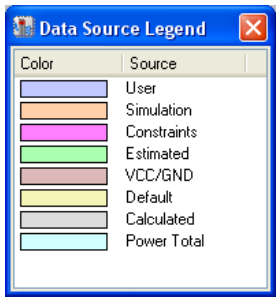
- Voltage Source Information

| Name | Power (W) | Voltage | Range | Icc (A) | Iccq (A) |
|---|---|---|---|---|---|
| Vccint | 0.66451 | 1.000 | 0.950 to 1.050 | 0.00000 | 0.66451 |
| Vccaux | 0.11250 | 2.500 | 2.375 to 2.625 | 0.00000 | 0.04500 |
| Vcco25 | 0.00250 | 2.500 | 2.380 to 2.630 | 0.00000 | 0.00100 |

| Name | Value | Range |
|---|---|---|
| FF Toggle Rate (%) | 15.0 | 0.0 to 200.0 |
| I/O Toggle Rate (%) | 15.0 | 0.0 to 200.0 |
| Output Load (pF) | 5.0 | 0.0 to 1000000.0 |
| I/O Enable Rate (%) | 100.0 | 0.0 to 100.0 |
| BRAM Write Rate (%) | 50.0 | 0.0 to 100.0 |
| BRAM Enable Rate (%) | 25.0 | 0.0 to 100.0 |
| DSP Toggle Rate (%) | 12.5 | 0.0 to 200.0 |
| | | |
| Part | xc6vlx75tff484-1 | |
| Package | ff484 | |
| Grade | Commercial | |
| Process | Typical | |

- Settings

- Each box is color coded



# Advanced Report

- Produced as a simple text file
  - File is given .pwr extension
  - Report is more detailed and stored in one text file
  - Some what-if analysis information is included
  - Includes a Power Improvement Guide

| Power summary | | I(mA) | P(mW) |
|---|---|---|---|
| Total estimated power consumption | | | 779.51 |
| Total Vccint | 1.00V | 664.51 | 664.51 |
| Total Vccaux | 2.50V | 45.00 | 112.50 |
| Total Vcco25 | 2.50V | 1.00 | 2.50 |
| Clocks | | | 0.00 |
| DSP | | | 0.00 |
| IO | | | 0.00 |
| Logic | | | 0.00 |
| Signals | | | 0.00 |
| Quiescent Vccint | 1.00V | 664.51 | 664.51 |
| Quiescent Vccaux | 2.50V | 45.00 | 112.50 |
| Quiescent Vcco25 | 2.50V | 1.00 | 2.50 |
| Package power limits, ambient 50C | | | 1891.89 |
| 250 LFM | | | 2713.18 |
| 500 LFM | | | 3070.18 |
| 750 LFM | | | 3333.33 |

| Thermal summary | |
|---|---|
| Estimated junction temperature | 53C |
| @ airflow of 250 LFM | 53C |
| 500 LFM | 53C |
| 750 LFM | 53C |
| Ambient temp | 50C |
| Case temp | 53C |
| Theta J-A | 4C/W |
| Max ambient at junction max of | 85C / 82C |
| 250 LFM | 82C |
| 500 LFM | 82C |
| 750 LFM | 82C |

# What Next?

- If you have a problem with your thermal budget there are many things you can consider
  - Determine which components in your design are using the most power
    - Try to use as much of the dedicated hardware as possible
  - Review the Power Improvement Guide section in the Advanced Power Report
  - Evaluate your activity rates
  - Reduce excess signal power or excess device utilization
    - Synthesis options
    - Implementation tool options
    - HDL code
    - Reduce excess static power
    - Adjust the external environment

# Summary

- Power calculations can be performed at three distinct phases of the design cycle
  - Concept phase: (Power Estimator spreadsheet)
  - Design phase: (XPower Analyzer)
  - System integration phase: (Lab measurements)
- Accurate power calculation at an early stage in the design cycle will result in fewer problems later
- The Power Estimator spreadsheet and the XPower Analyzer can be used for estimating the power consumption and the junction temperature of all Xilinx FPGA and CPLD devices
- The Power Estimator and XPower Analyzer uses activity rates to calculate total average power consumption

# Where Can I Learn More?

- Command Line Tools User Guide: XPower chapter
  - **Help → Software Manuals → Command Line Tools User Guide**
- Online help from the XPower GUI
- Xilinx Power Solutions Web Page
  - **www.support.xilinx.com → Technology Solutions → Power Solutions**
  - Get the XPower Estimator spreadsheets for all Xilinx devices
  - *7 Steps to Worst Case Power Estimation*, WP353
  - *Spartan-6 Power Management User Guide*, UG394
  - *Power Consumption at 40 and 45 nm*, 298
- Application Notes: **Help → Xilinx on the Web → Xilinx Application Notes**
  - Application Note XAPP158: *Powering Xilinx FPGAs*
- **Xilinx Training**
  - **www.xilinx.com/training**
    - Xilinx tools and architecture courses
    - Hardware description language courses
    - Basic FPGA architecture and other topics (free training videos)

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