CMPE 650 – Homework/Project #2

This project is for processing (Convert an RGB image to grayscale image) a128x128 pixel image on FPGA and displaying it from FPGA to monitor using a VGA port.

The project consists of three parts:
1. Store data on FPGA
    - Store data (Pixel values of an image) on FPGA ROM
2. Processing by FPGA
    - Convert image from colored to grayscale
3. Display processed image from FPGA to a monitor though VGA

Detail Description

1. Use MATLAB to obtain matrix of pixels of a colored image that you find (example given for an 128x128 image) and desired output matrix (You will use origImageData to process on FPGA and after that you should get output matching to newImageData. Keep in mind newImageData obtained from Matlab is just for a verification purpose, you should be getting these values as an output from your Verilog code)
The following Matlab function is provided:
imageRGB2BW():
DESCRIPTION: Converts image from RGB to grayscale in MATLAB
INPUTS:
    - imageFile: The location of the source image file to convert
OUTPUTS:
    - origImageData: Matrix representation of source image
    - newImageData: Matrix representation of destination image

2. For FPGA implementation you need to design the RGB to B&W conversion and access the VGA port on board:
    - RGB to B&W conversion, every pixel consists of three element (Red, Green and Blue) to convert to Black and White you need to replace red, green & blue values with this normalized sum:

        0.21*Red + 0.71*Green + 0.07*Blue

    new_pixel(i,j).red = pixel(i,j).red + pixel(i,j).green + pixel(i,j).blue;
    new_pixel(i,j).green = pixel(i,j).red + pixel(i,j).green + pixel(i,j).blue;
    new_pixel(i,j).blue = pixel(i,j).red + pixel(i,j).green + pixel(i,j).blue;

You need to implement the coefficient multiplication by the closest value.

• For FPGA implementation and test, you need to define the pins in the UCF file just like mentioned in the counter example in the tutorial provided.

What to submit

Fully tested design with testbench and hardware demonstration

1. Phase 1: Verified design in simulation
    - First get the RGB-BW part in FPGA working by a simple testbench
    - Note that each design module must be accompanied by a testbench and be verified.

2. Phase 2: Verified design in Hardware and demonstration
    - Then access the VGA port to send data to the monitor and show the original and black and white on monitor
    - Major portion of grade is based on successful hardware demonstration

3. Phase 1 and Phase 2: A Report of your design and detailed block diagrams of your design and statement of which parts are working.