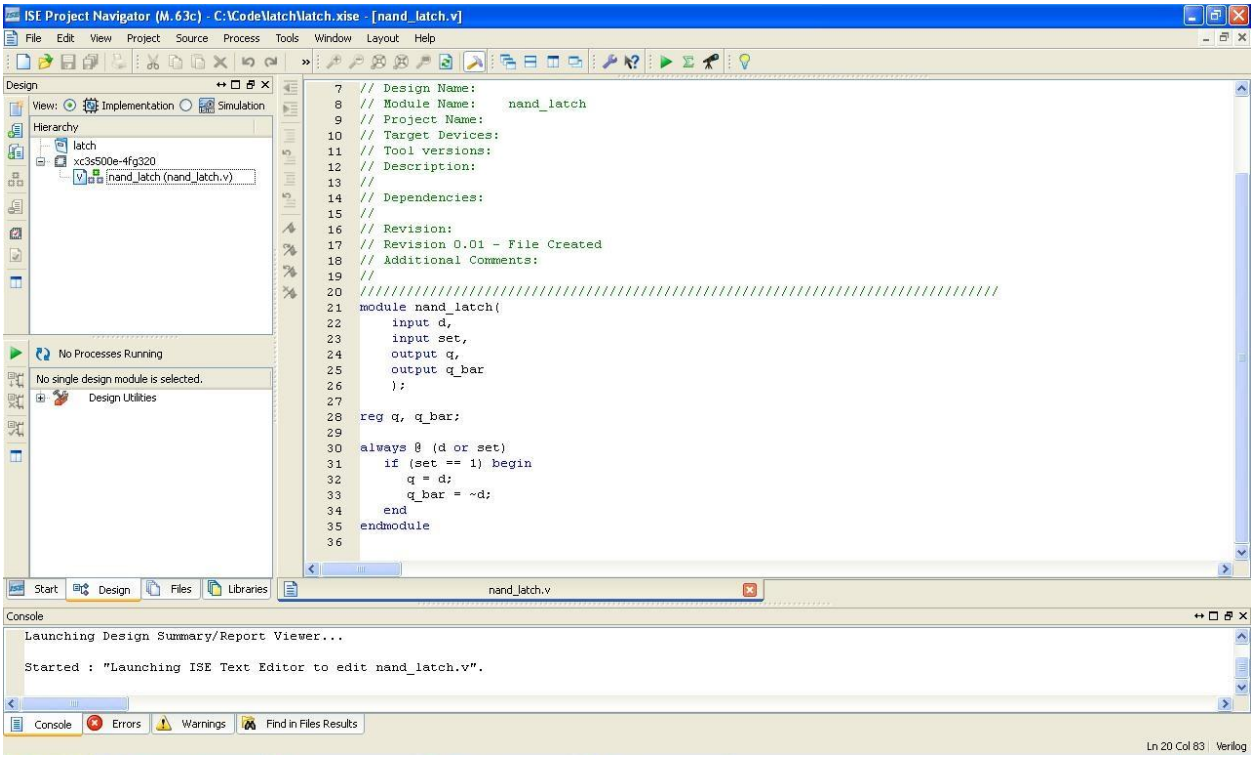
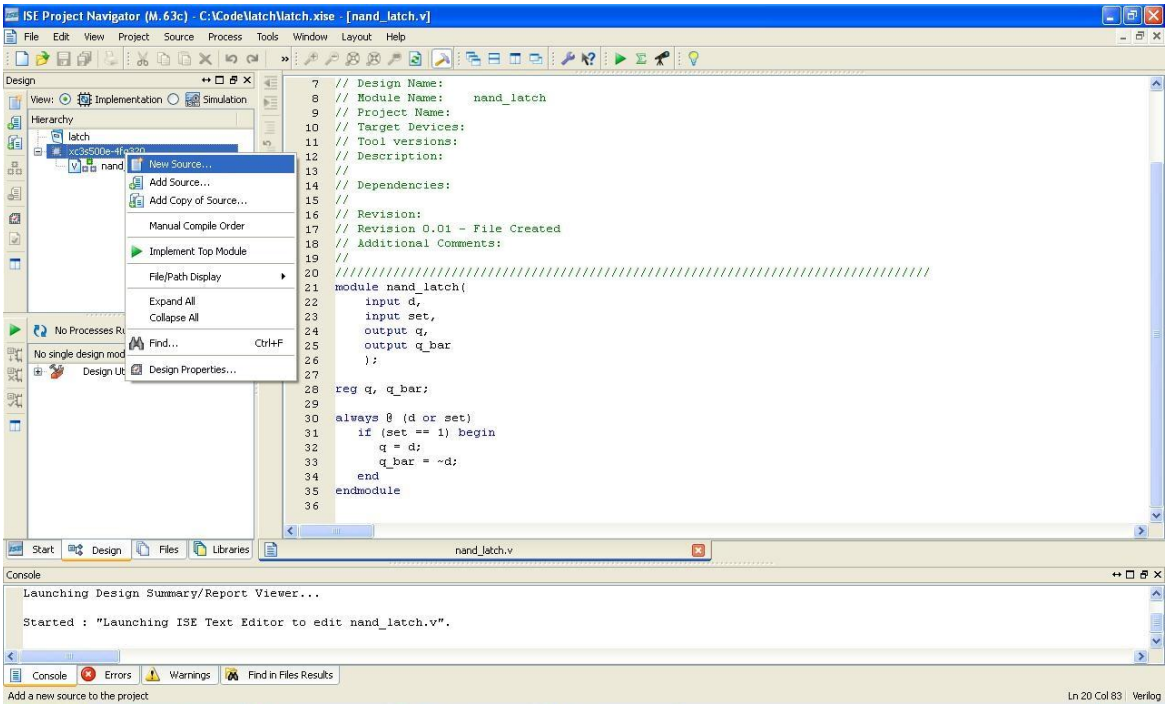
ISim Testbench Tutorial

ISIM or the ISE Simulator allows you to analyze and debug your code. This tutorial will show you how to write a simple testbench for your module and run the simulation using ISim.

1. First open your project with the top level module that you want to test.

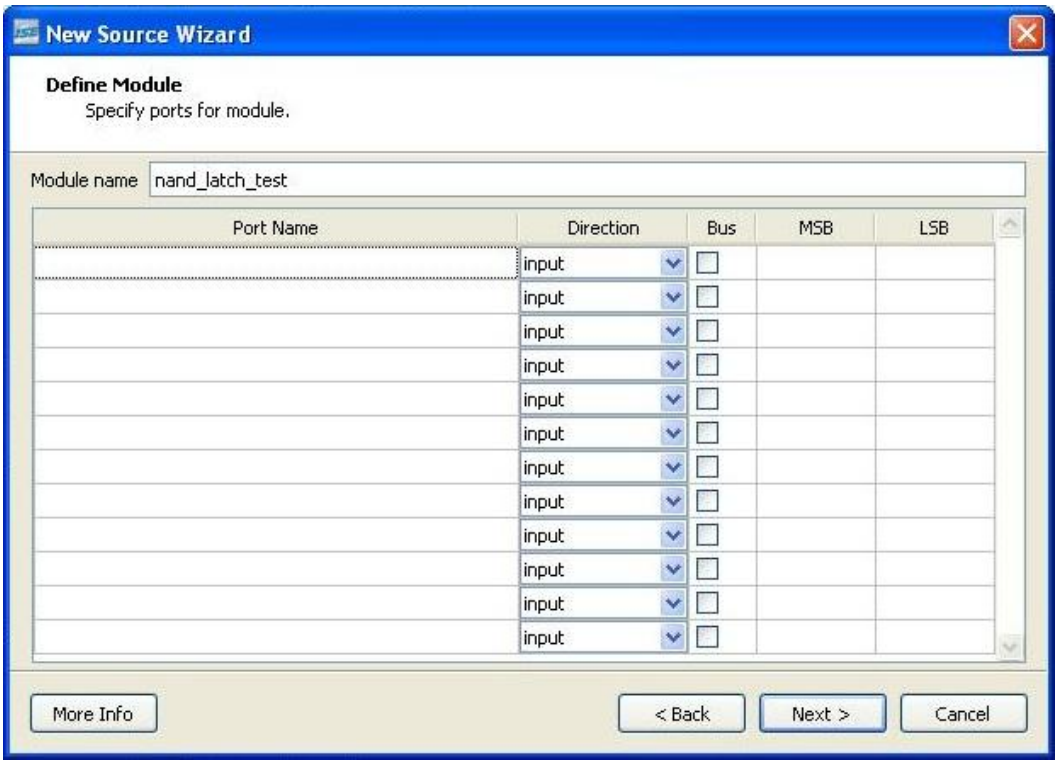


2. Next we need to create the testbench for this design. Add a new source to the design

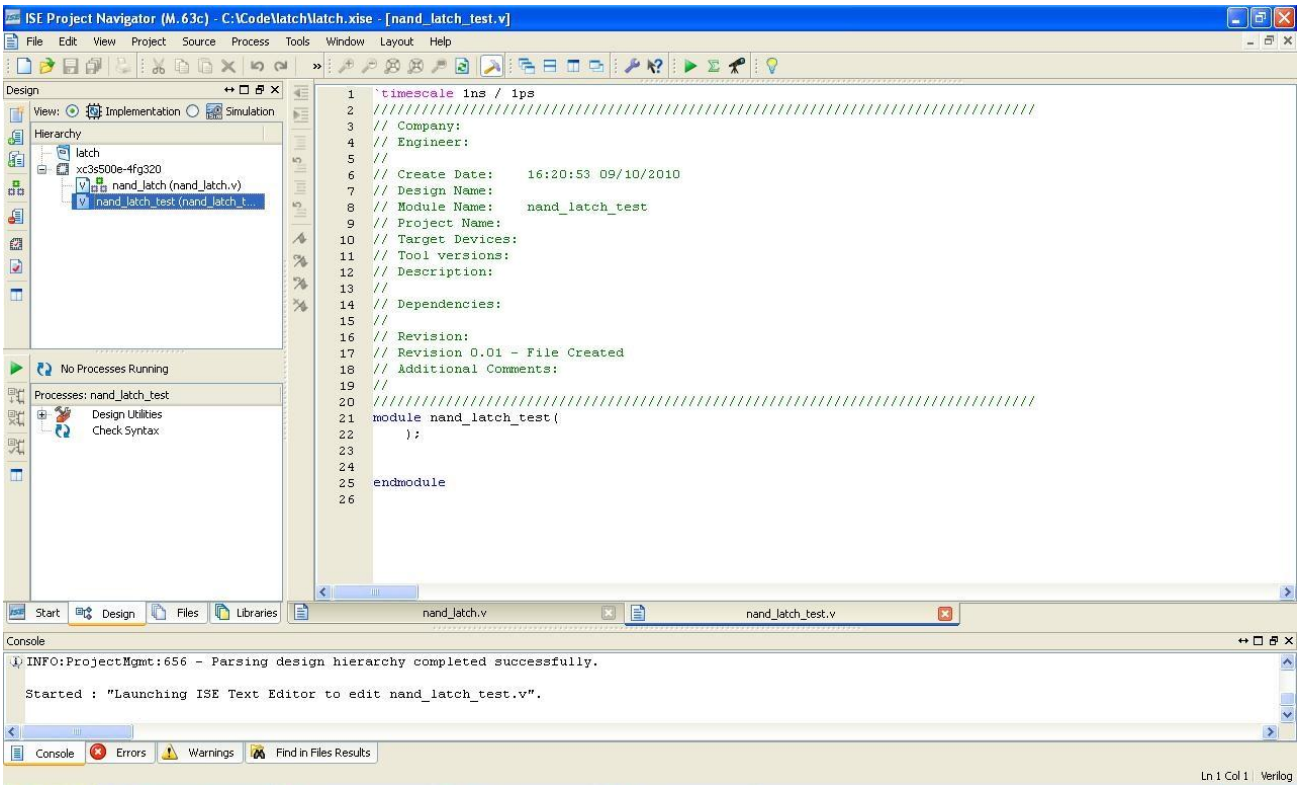


3. Select Verilog Module and name your testbench.

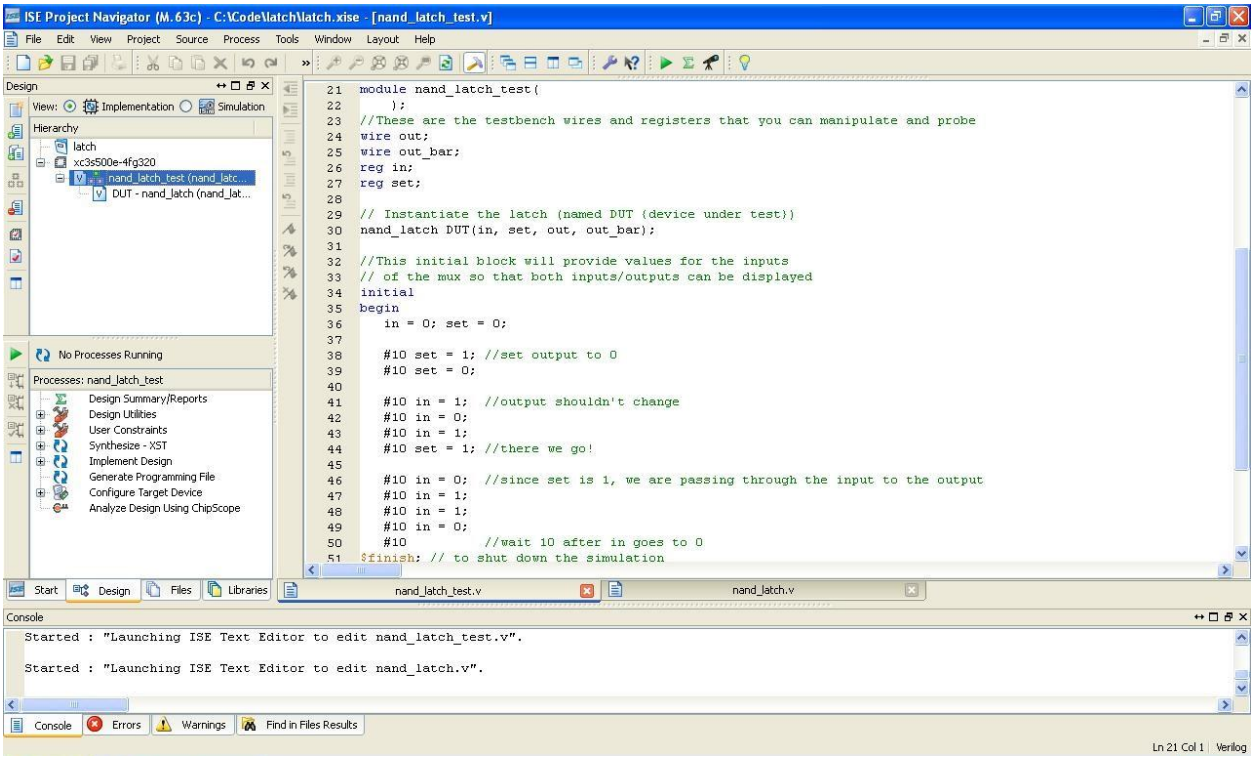
4. The testbench does not require any inputs or outputs so you can ignore the ports window.



5. This is what your project window should look like after adding your testbench.

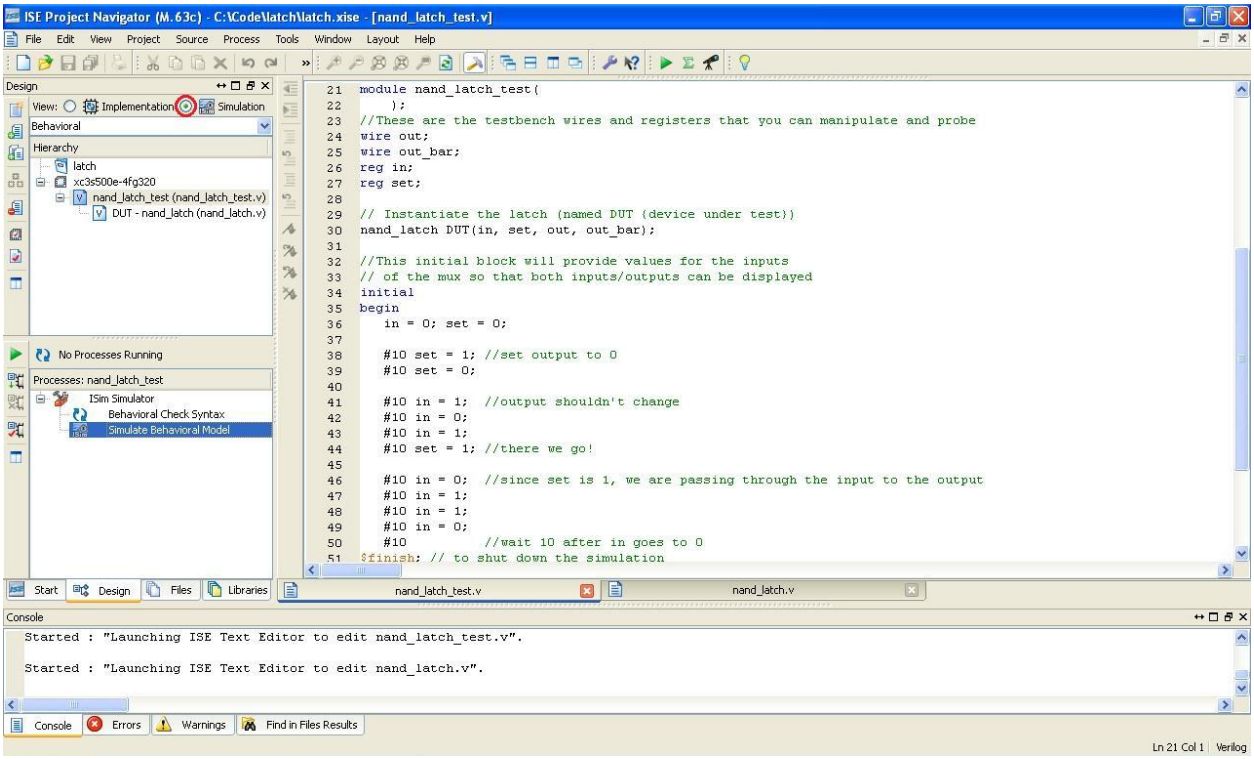


6. Next create your testbench. After you save it your project should look like this.




```
21  module nand_latch_test(
22      );
23  //These are the testbench wires and registers that you can manipulate and probe
24  wire out;
25  wire out_bar;
26  reg in;
27  reg set;
28
29  // Instantiate the latch (named DUT (device under test))
30  nand_latch DUT(in, set, out, out_bar);
31
32  //This initial block will provide values for the inputs
33  // of the mux so that both inputs/outputs can be displayed
34  initial
35  begin
36     in = 0; set = 0;
37
38     #10 set = 1; //set output to 0
39     #10 set = 0;
40
41     #10 in = 1;  //output shouldn't change
42     #10 in = 0;
43     #10 in = 1;
44     #10 set = 1; //there we go!
45
46     #10 in = 0;  //since set is 1, we are passing through the input to the output
47     #10 in = 1;
48     #10 in = 1;
49     #10 in = 0;
50     #10          //wait 10 after in goes to 0
51  $finish; // to shut down the simulation
```

7. Inside the design area select the simulation radial button (circled in red). Select your testbench and double click simulate behavioral model.

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8. ISim will launch and from here you can look at your waveform to debug your top level module. Anything set to display to the console will be saved in “isim.txt” in your project folder.