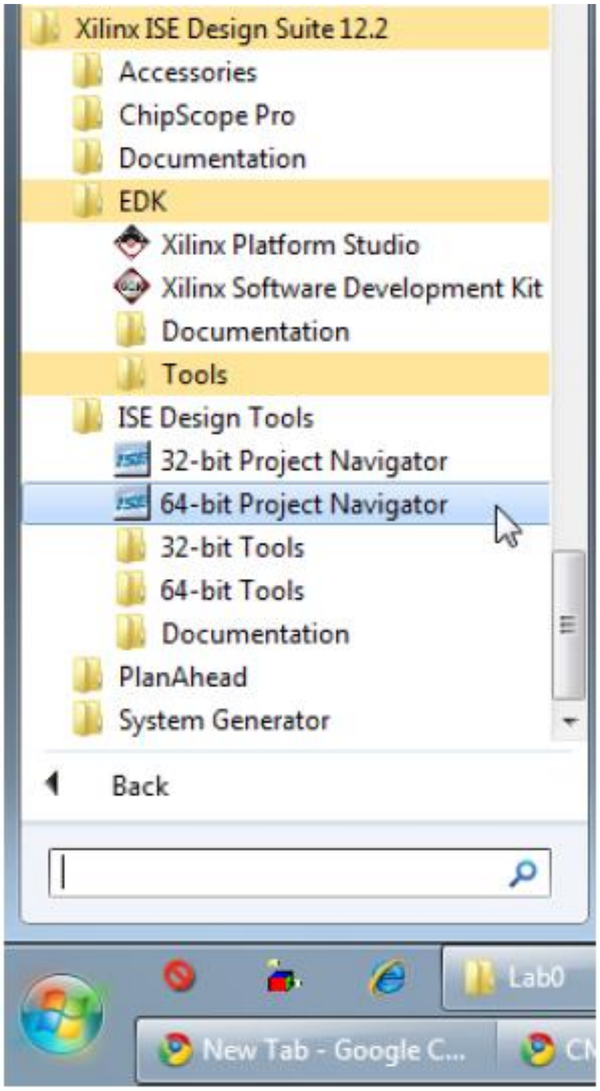
Verilog Module Tutorial

By TA Brian W. Stevens – CMPE415 – UMBC Spring 2015 – Dr. Tinoosh Mohsenin

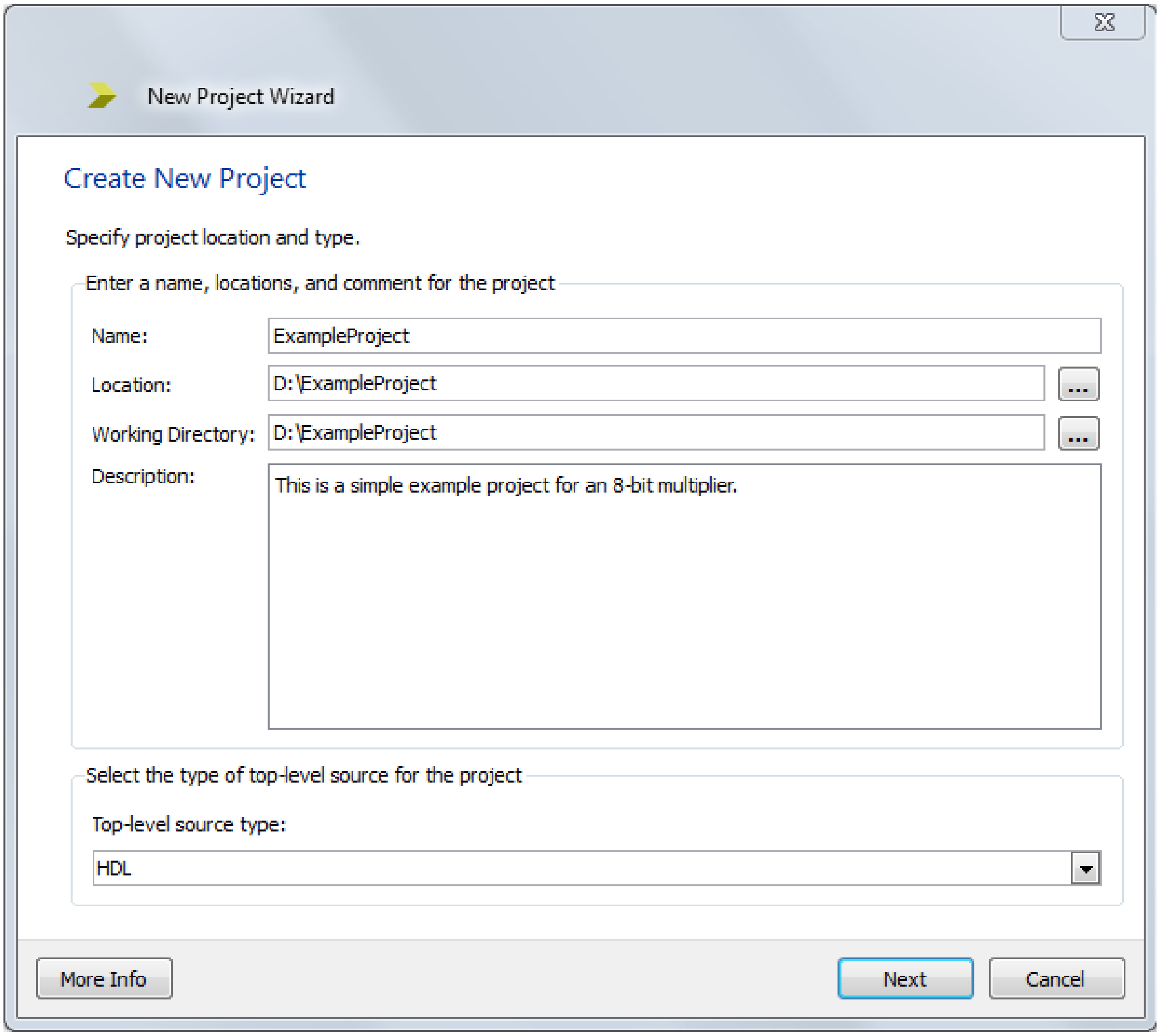
What will this guide teach you?

This guide will go through how to use Xilinx 13.2 to create a Verilog module for a simple 8 bit multiplier. It will show you how to add files to Xilinx projects and how to incorporate a testbench for your Verilog module. There are also some other helpful tips as well.

1. **Open up Xilinx ISE Design Suite 13.2**



2. **Create New Project**
   a. On the top toolbar go to File > New Project
   b. Name your project and select the location for the project



Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: ExampleProject

Location: D:\ExampleProject

Working Directory: D:\ExampleProject

Description: This is a simple example project for an 8-bit multiplier.

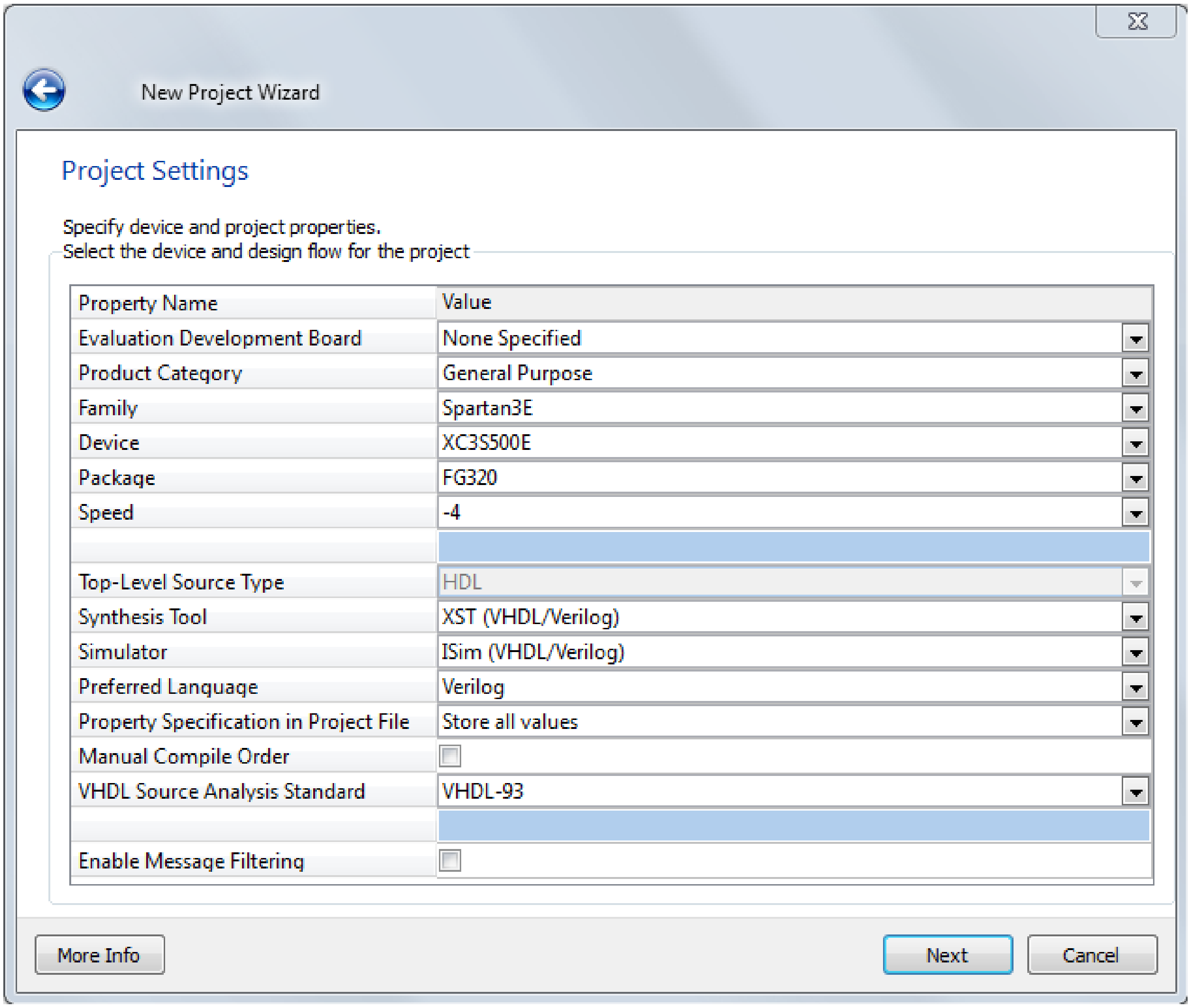
Select the type of top-level source for the project

Top-level source type: HDL

   c. Click Next

3. **Project Settings**

   a. Enter the following information about your FPGA. This information is also under "Spartan-3E FPGA Family: Data Sheet" under Package Marking (page 6). http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf



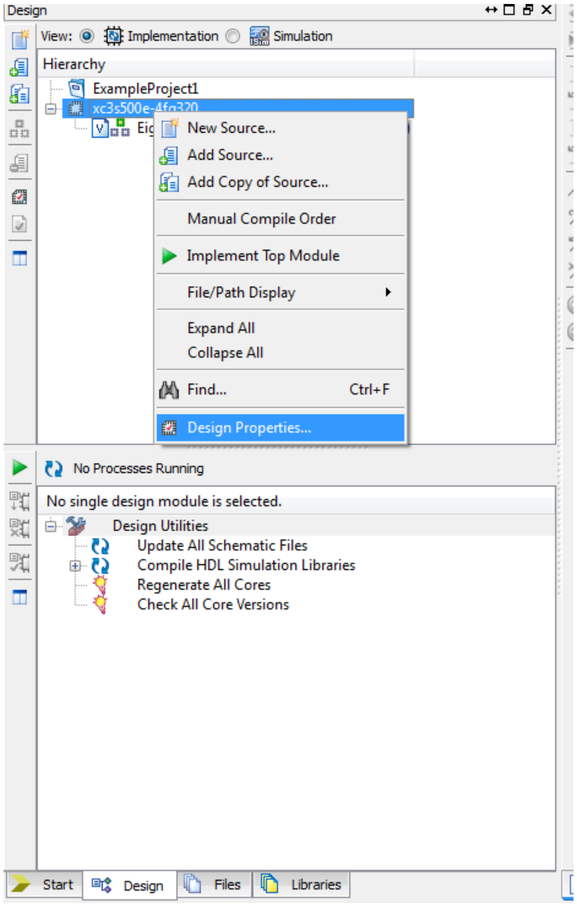
Project Settings

Specify device and project properties.
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	General Purpose
Family	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	□
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	□

   b. Click Next

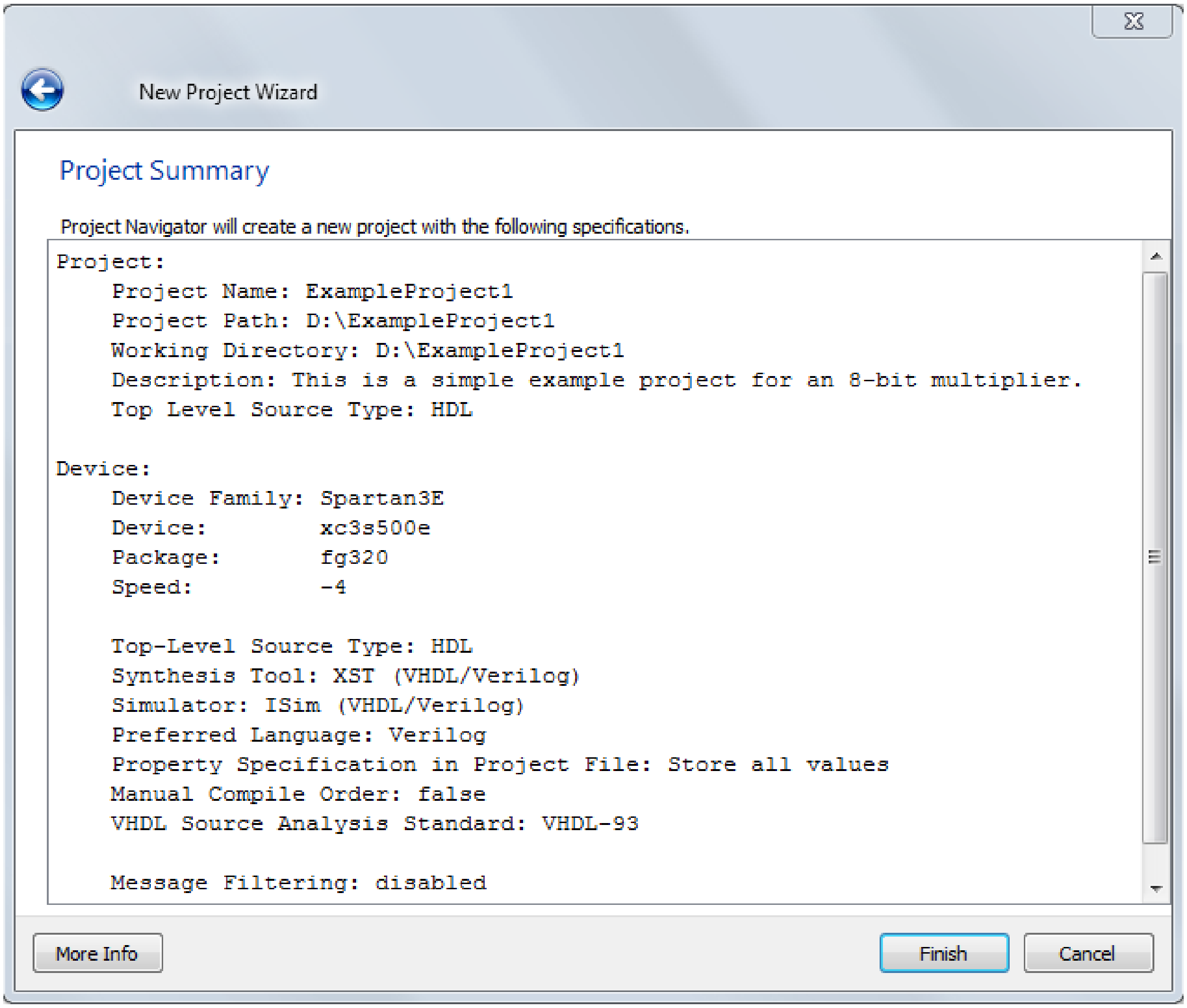
- Helpful Hint #2 – you can change the settings of your FPGA Board(Speed, Family, Package… ect) by right clicking your project tree and selecting “Design Properties”



No Processes Running

No single design module is selected.

4. **Project Summary Displayed**



Project Summary

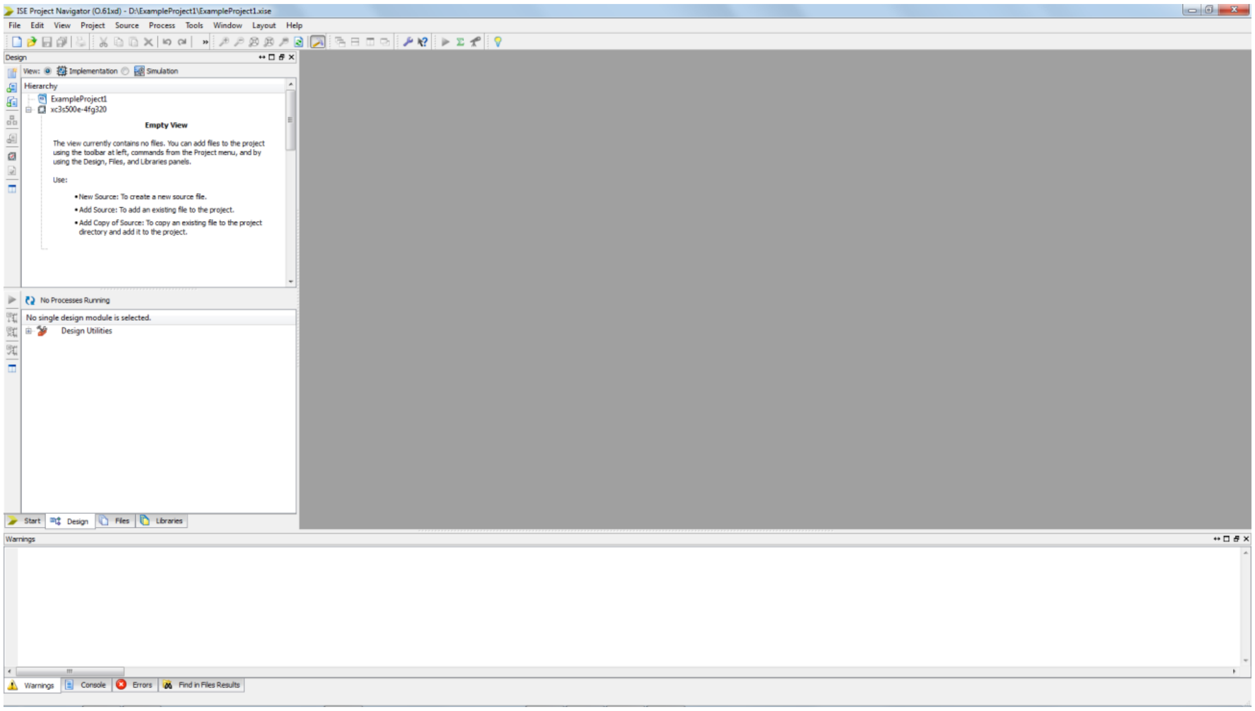
Project Navigator will create a new project with the following specifications.

```
Project:
    Project Name: ExampleProject1
    Project Path: D:\ExampleProject1
    Working Directory: D:\ExampleProject1
    Description: This is a simple example project for an 8-bit multiplier.
    Top Level Source Type: HDL

Device:
    Device Family: Spartan3E
    Device:        xc3s500e
    Package:       fg320
    Speed:         -4

    Top-Level Source Type: HDL
    Synthesis Tool: XST (VHDL/Verilog)
    Simulator: ISim (VHDL/Verilog)
    Preferred Language: Verilog
    Property Specification in Project File: Store all values
    Manual Compile Order: false
    VHDL Source Analysis Standard: VHDL-93

    Message Filtering: disabled
```

a. Click Finish

5. Project ISE Display

a. Your project environment will be displayed as seen below.


ISE Project Navigator (O.61xd) - D:\ExampleProject1\ExampleProject1.xise
File Edit View Project Source Process Tools Window Layout Help
Design
View: ● Implementation ○ Simulation
Hierarchy
ExampleProject1
xc3s500e-4fg320
No Processes Running
Design Utilities
Start Design Files Libraries
Warnings
Warnings Console Errors Find in Files Results

Empty View

The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.

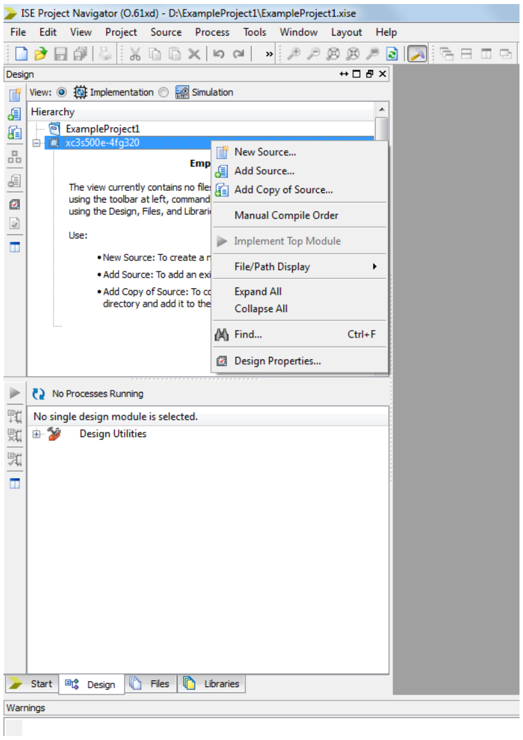
Use:

- New Source: To create a new source file.
- Add Source: To add an existing file to the project.
- Add Copy of Source: To copy an existing file to the project directory and add it to the project.

No single design module is selected.

6. Create a New Source

a. Right click on the project and select “New Source” as seen below **OR** go to Project > New Source **OR** you can use the buttons to the left of the hierarchy tree

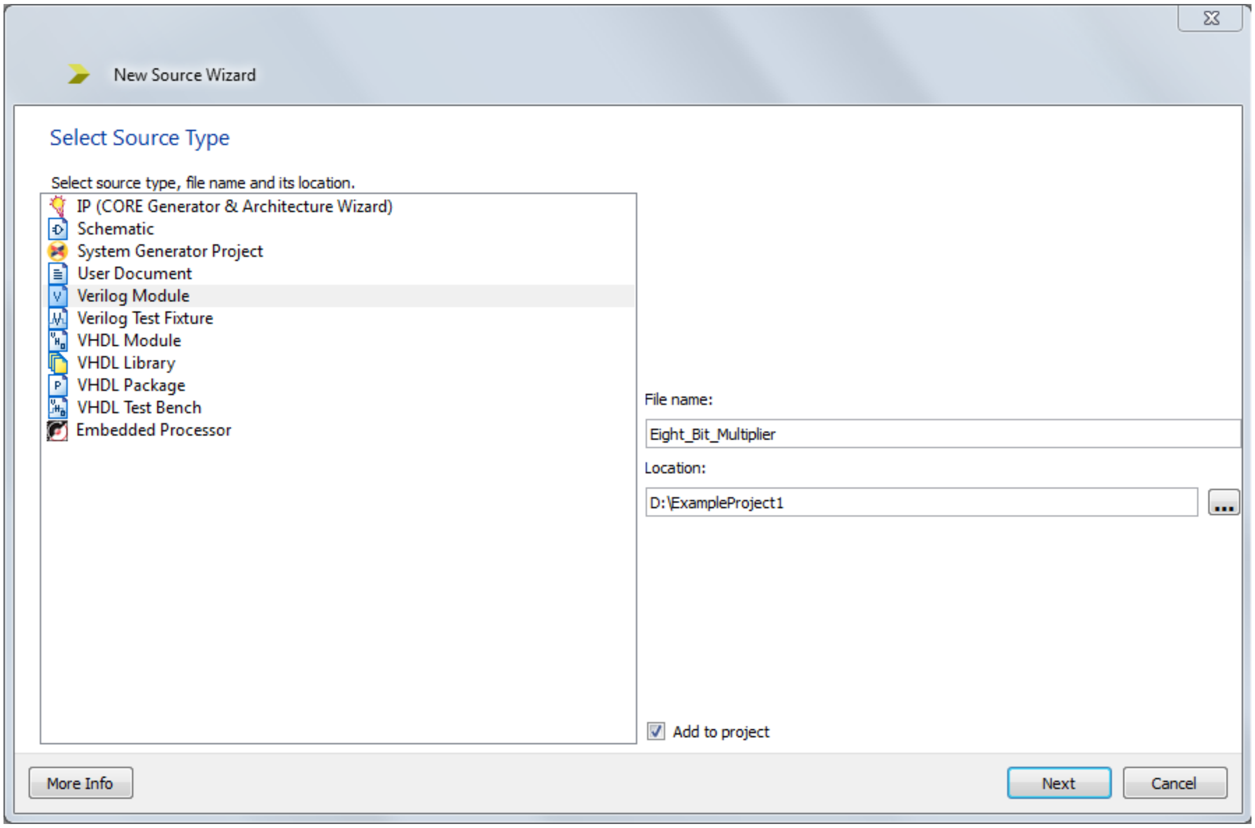


No single design module is selected.

- Helpful Tip #1 – here you can also add existing Verilog and other source files to your design, here are the options
    a. New Source - starts wizard to create a new source file (Verilog, VHDL, Schematic, etc...), creating a shell if desired, and adds it for use in the project.
    b. Add Source - Allows you to point to a source file in the project directory or anywhere else and include it for use in the project
    c. Add Copy of Source - Creates a copy of the source file in the project directory and adds the copy for use in the project

7. New Source Type and File Name

   a. After clicking “New Source”, select “Verilog Module” as the file type and enter the file name(here as “Eight_Bit_Multipler”) as seen below.



New Source Wizard

Select Source Type

Select source type, file name and its location.

- IP (CORE Generator & Architecture Wizard)
- Schematic
- System Generator Project
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench
- Embedded Processor

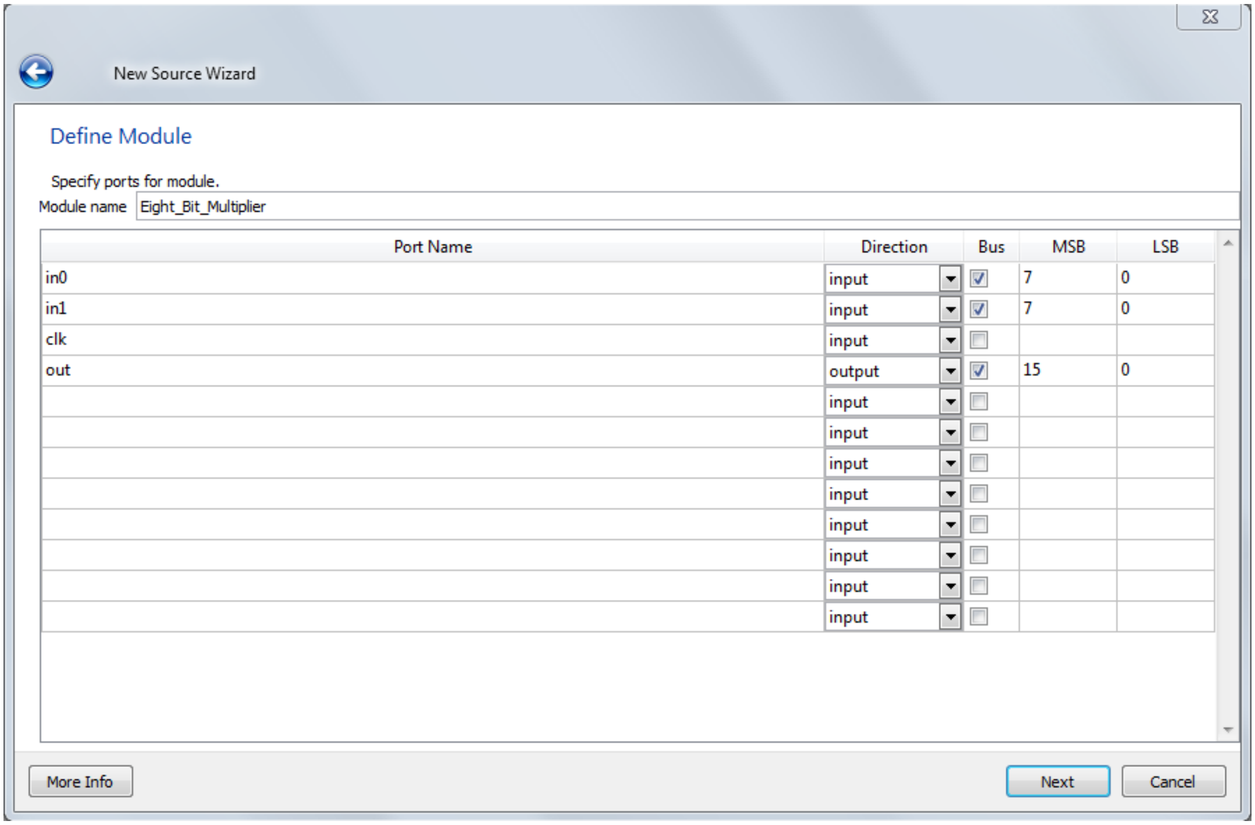
File name: Eight_Bit_Multiplier

Location: D:\ExampleProject1

☑ Add to project

8. **Pre-define Inputs and Outputs**

   a. This window allows you to enter in your pre-defined inputs and outputs. This step will automatically create a template module for you with the inputs and outputs you type below. However, this is not required and you can always just select "Next" and change the inputs and outputs later.



Define Module

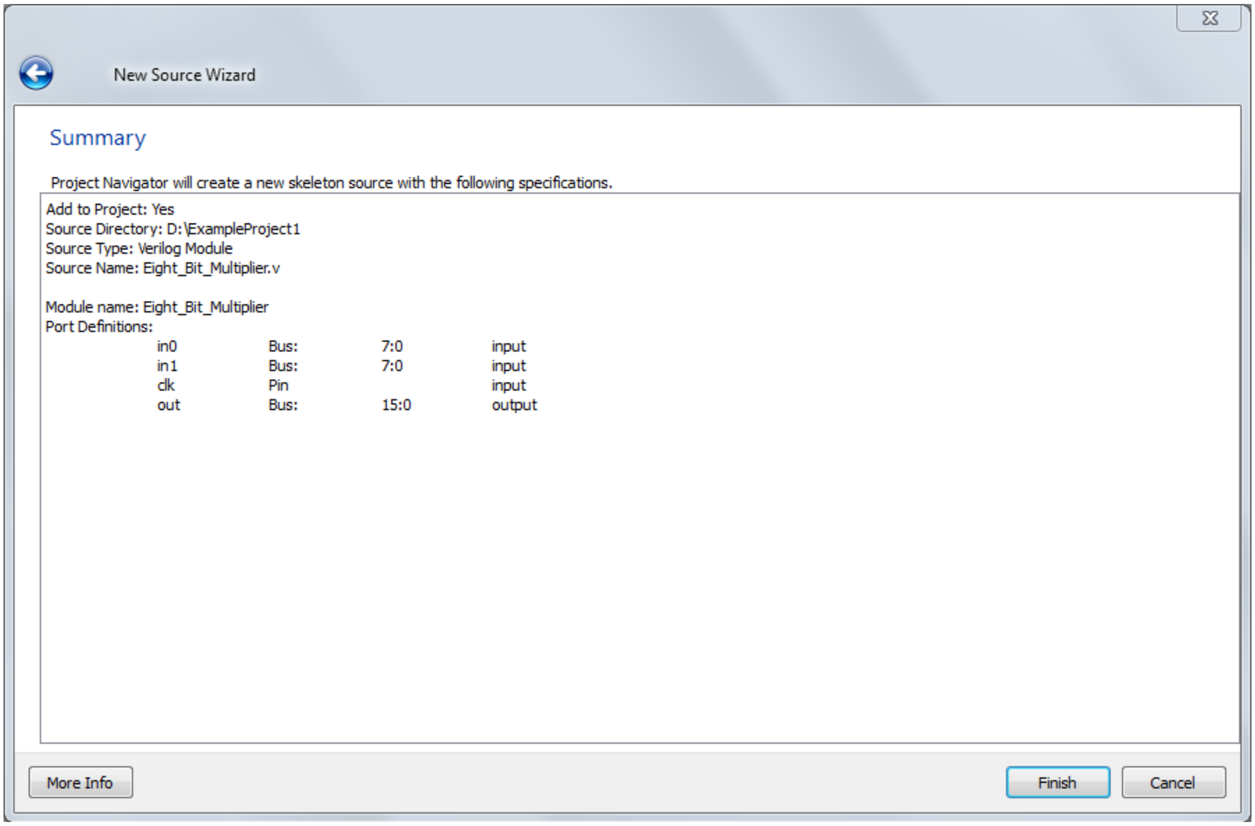
Specify ports for module.

Module name Eight_Bit_Multiplier

Port Name	Direction	Bus	MSB	LSB
in0	input	☑	7	0
in1	input	☑	7	0
clk	input	□		
out	output	☑	15	0
	input	□		
	input	□		
	input	□		
	input	□		
	input	□		
	input	□		
	input	□		
	input	□		

   b. Click Next

9. **Summary Displayed**
    a. Displays a summary of the file you are creating, lists inputs/outputs ect.



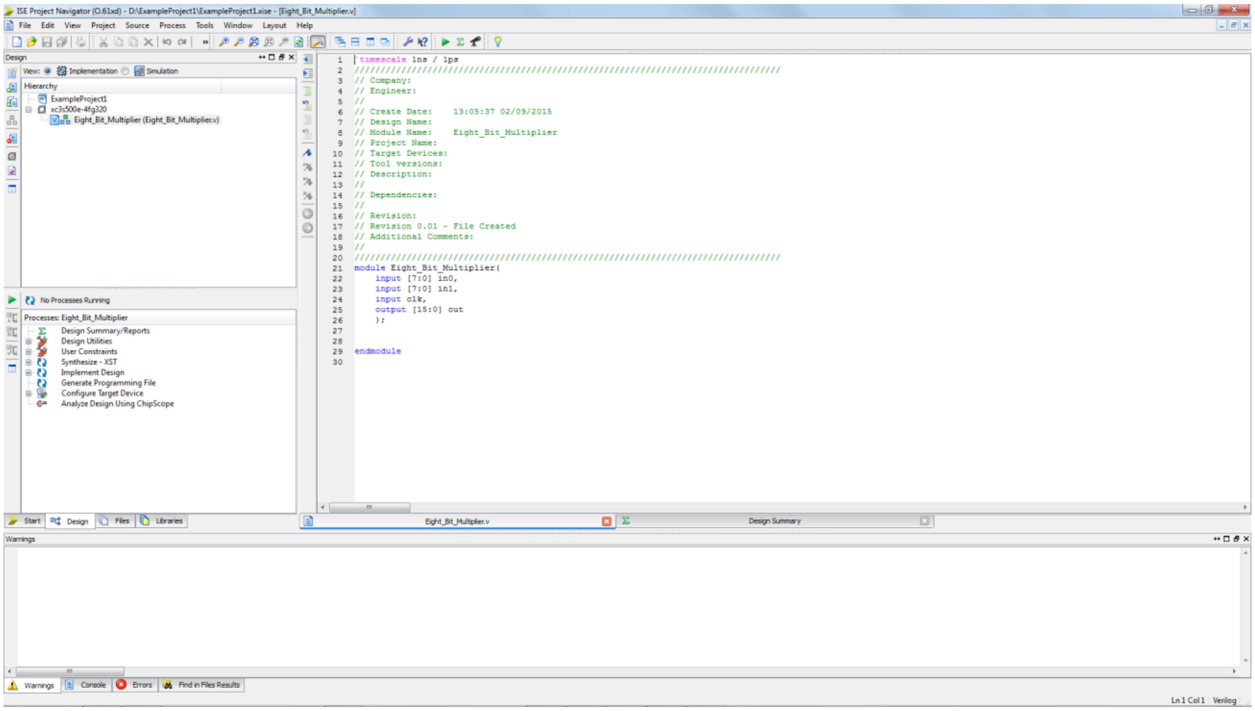
Project Navigator will create a new skeleton source with the following specifications.

```
Add to Project: Yes
Source Directory: D:\ExampleProject1
Source Type: Verilog Module
Source Name: Eight_Bit_Multiplier.v

Module name: Eight_Bit_Multiplier
Port Definitions:
                in0         Bus:        7:0         input
                in1         Bus:        7:0         input
                clk         Pin                     input
                out         Bus:        15:0        output
```

    b. Click Finish

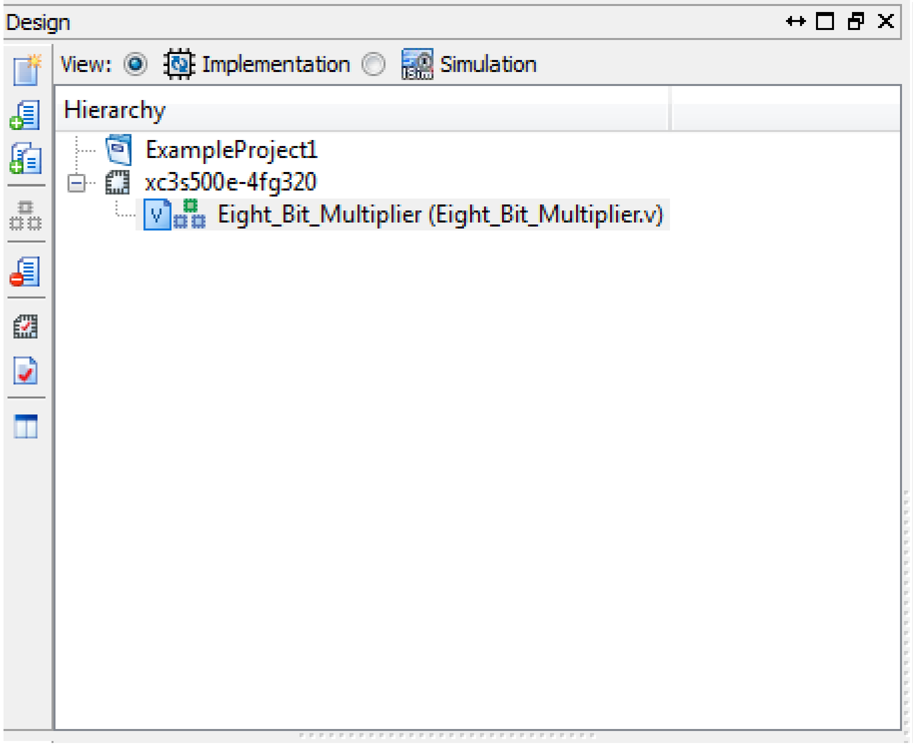
10. New Verilog File Displayed

a. This will now show your added file in the ISE environment.

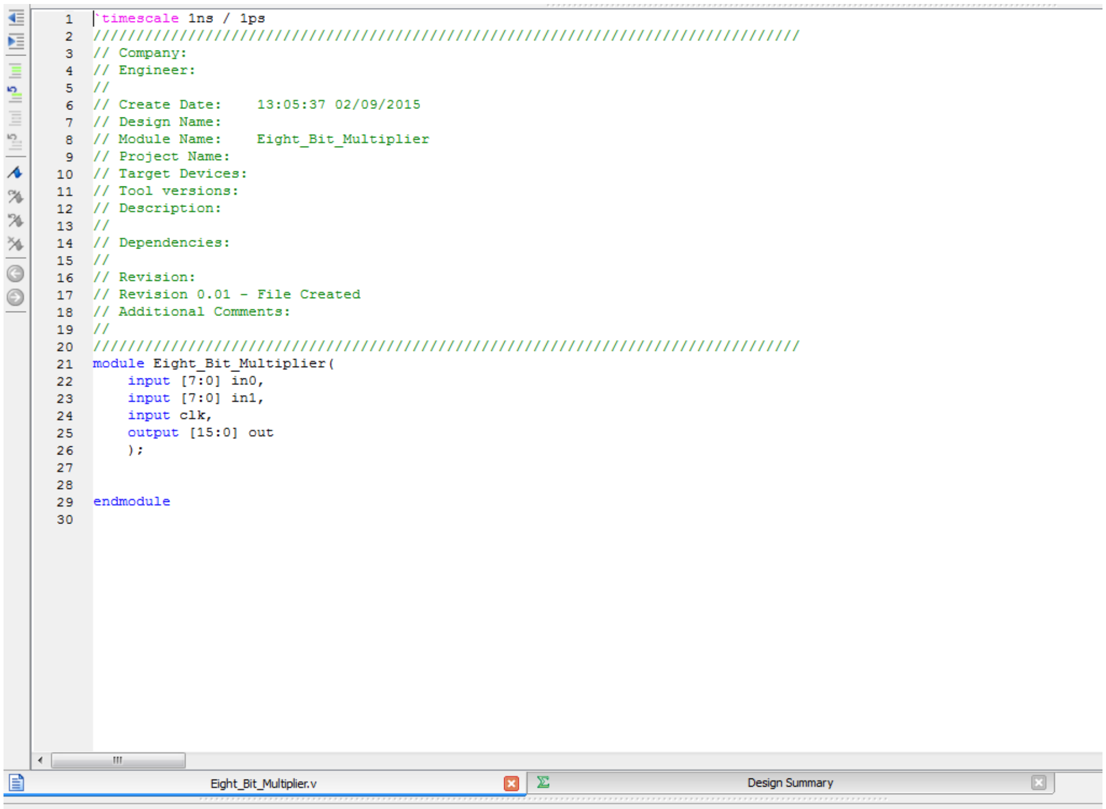


```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:05:37 02/09/2015
// Design Name:
// Module Name:    Eight_Bit_Multiplier
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Eight_Bit_Multiplier(
    input [7:0] in0,
    input [7:0] in1,
    input clk,
    output [15:0] out
    );


endmodule
```

b. You will notice that the Verilog module has been added under your project tree(hierarchy)

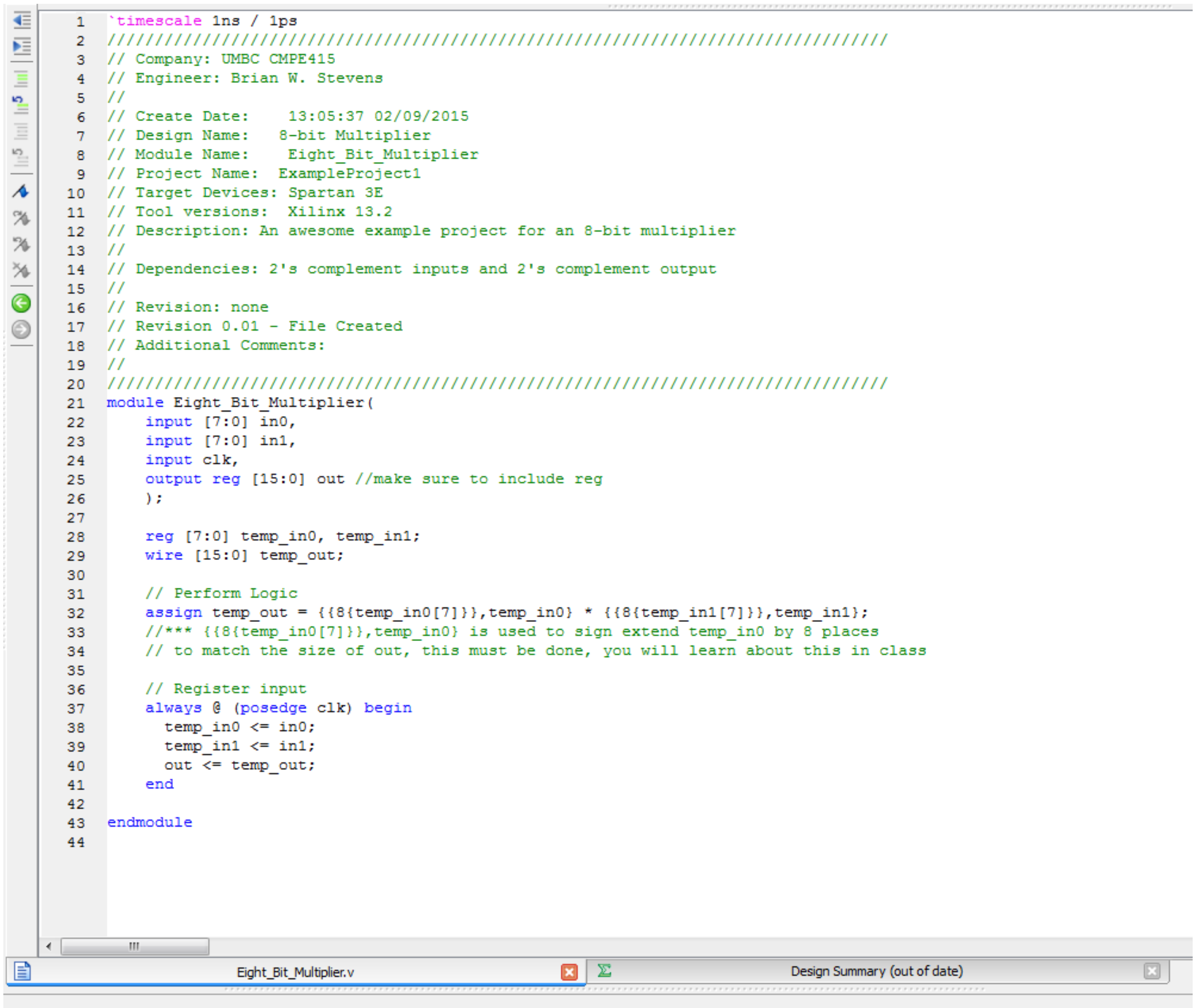


c. Your new file will show your auto-generated Verilog module with any inputs and outputs already previously defined.



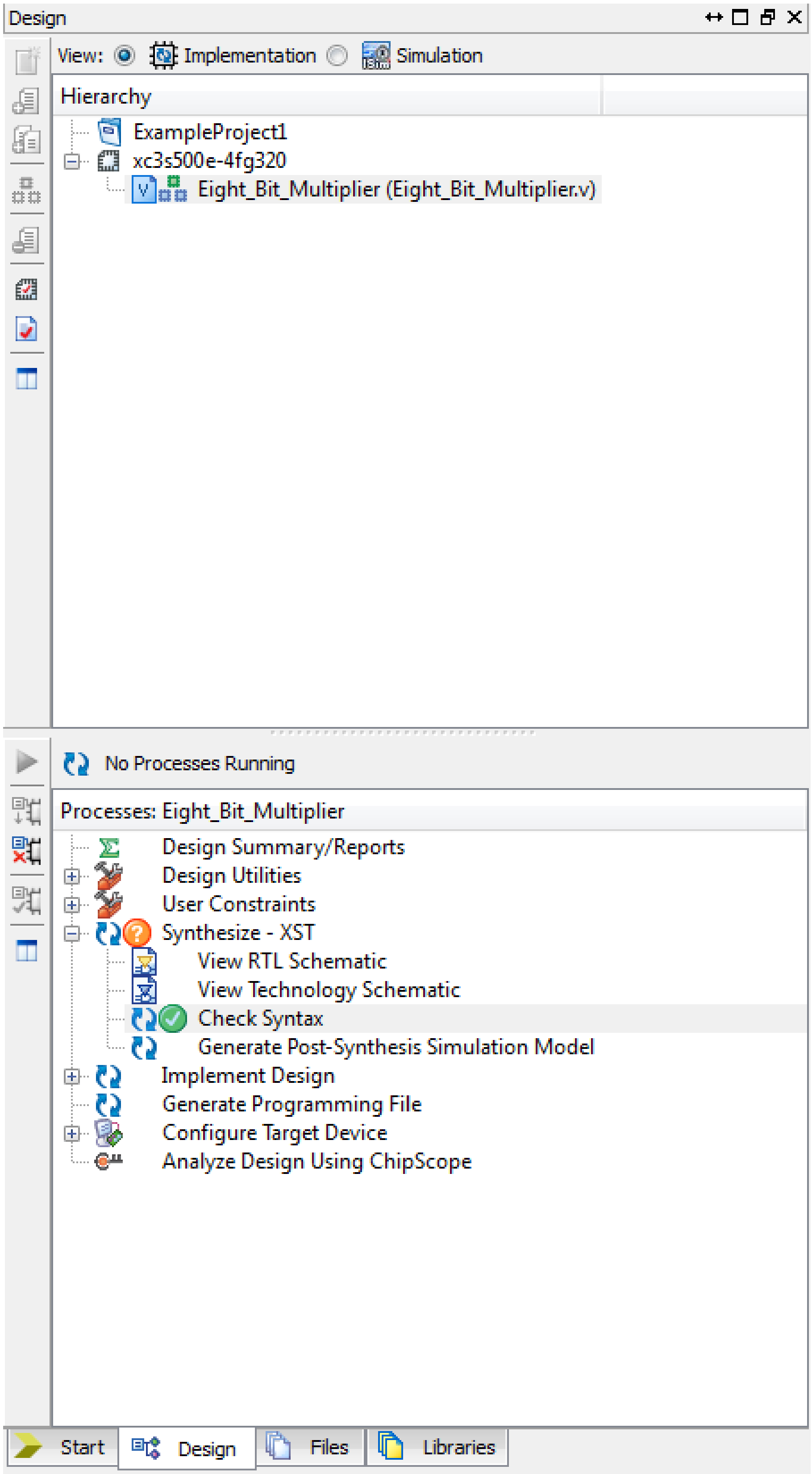
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:05:37 02/09/2015
// Design Name:
// Module Name:    Eight_Bit_Multiplier
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Eight_Bit_Multiplier(
    input [7:0] in0,
    input [7:0] in1,
    input clk,
    output [15:0] out
    );


endmodule
```

d. Completed code for the 8-bit multiplier is below. You will learn about this syntax in class.



```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company: UMBC CMPE415
// Engineer: Brian W. Stevens
//
// Create Date:    13:05:37 02/09/2015
// Design Name:   8-bit Multiplier
// Module Name:    Eight_Bit_Multiplier
// Project Name:  ExampleProject1
// Target Devices: Spartan 3E
// Tool versions:  Xilinx 13.2
// Description: An awesome example project for an 8-bit multiplier
//
// Dependencies: 2's complement inputs and 2's complement output
//
// Revision: none
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Eight_Bit_Multiplier(
    input [7:0] in0,
    input [7:0] in1,
    input clk,
    output reg [15:0] out //make sure to include reg
    );

    reg [7:0] temp_in0, temp_in1;
    wire [15:0] temp_out;

    // Perform Logic
    assign temp_out = {{8{temp_in0[7]}},temp_in0} * {{8{temp_in1[7]}},temp_in1};
    //*** {{8{temp_in0[7]}},temp_in0} is used to sign extend temp_in0 by 8 places
    // to match the size of out, this must be done, you will learn about this in class

    // Register input
    always @ (posedge clk) begin
      temp_in0 <= in0;
      temp_in1 <= in1;
      out <= temp_out;
    end

endmodule
```

e. Make sure to check syntax before running simulations of your Verilog modules

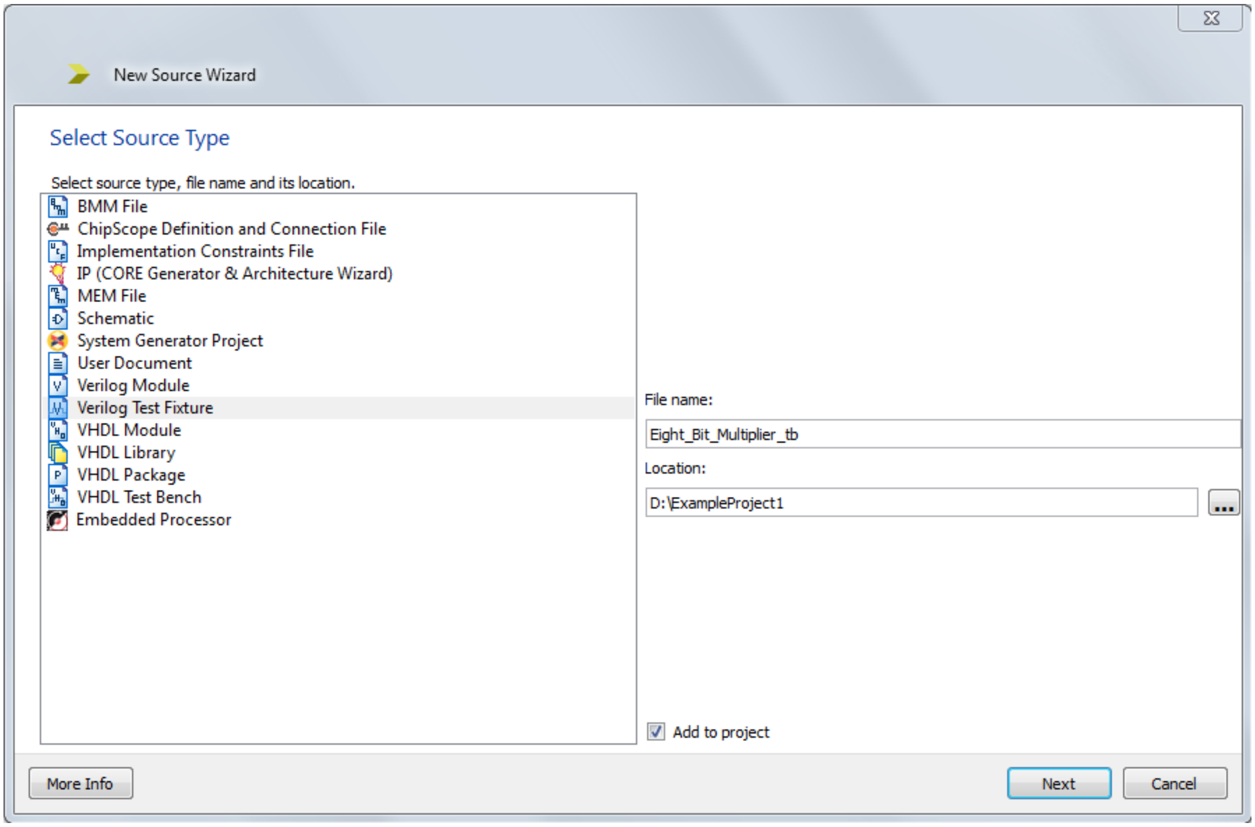

Design
View: ● Implementation ○ Simulation
Hierarchy
ExampleProject1
xc3s500e-4fg320
Eight_Bit_Multiplier (Eight_Bit_Multiplier.v)
No Processes Running
Processes: Eight_Bit_Multiplier
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start
Design
Files
Libraries

11. Creating a Testbench

a. Now we will create a testbench based off our Verilog module

b. Go to Project > New Source

c. Select Verilog Test Fixture and name the file with an extension such as "_tb" or "_test"



Select Source Type

Select source type, file name and its location.

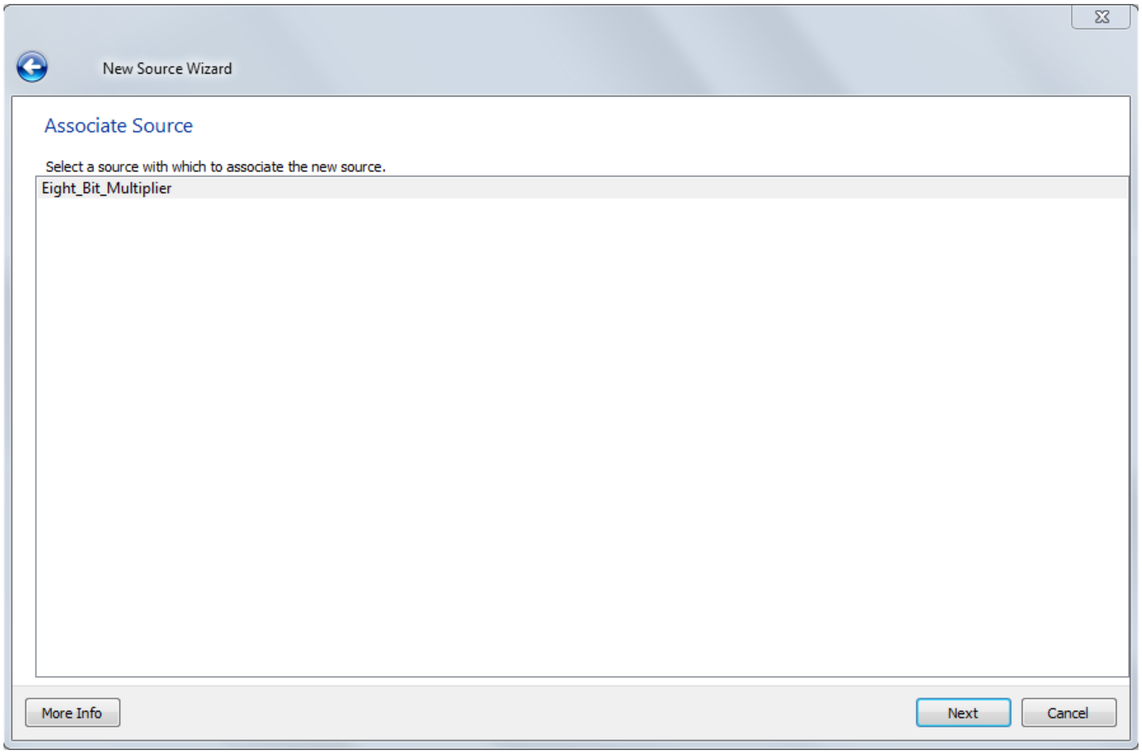
- BMM File
- ChipScope Definition and Connection File
- Implementation Constraints File
- IP (CORE Generator & Architecture Wizard)
- MEM File
- Schematic
- System Generator Project
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench
- Embedded Processor

File name: Eight_Bit_Multiplier_tb

Location: D:\ExampleProject1

☑ Add to project

d. Choose the associate source or the Verilog file you wish to make a testbech for.



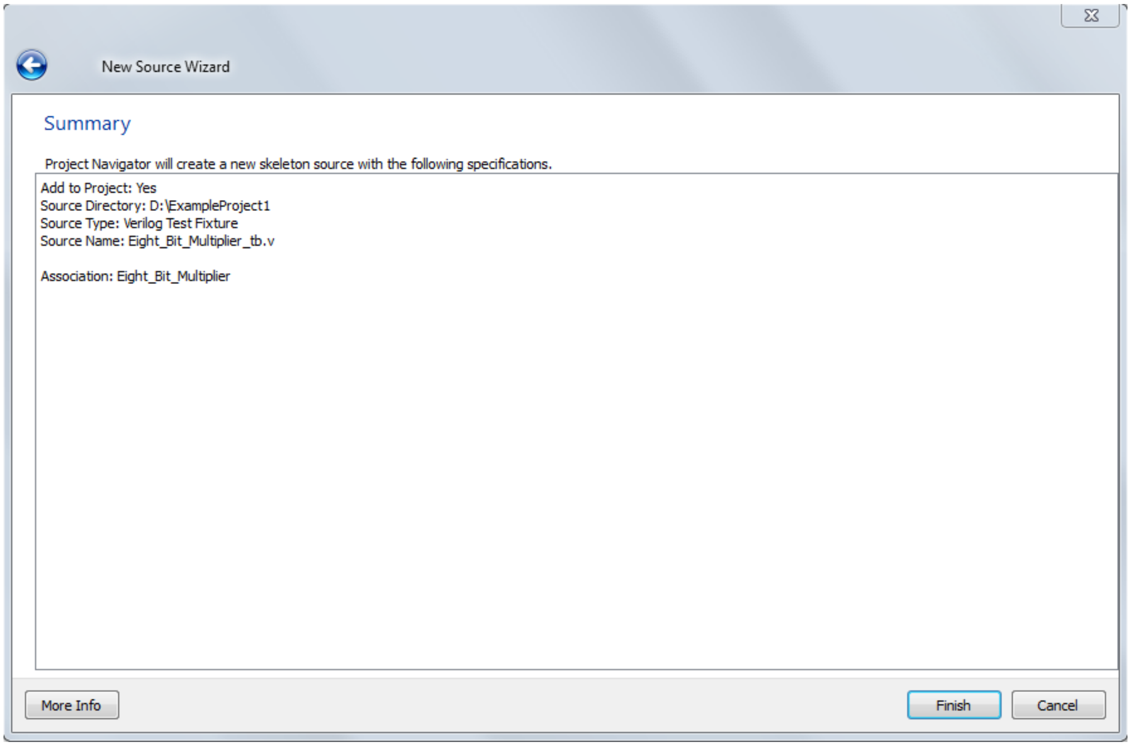
Associate Source

Select a source with which to associate the new source.

Eight_Bit_Multiplier

e. Click Next

12. Summary of Testbench



Summary

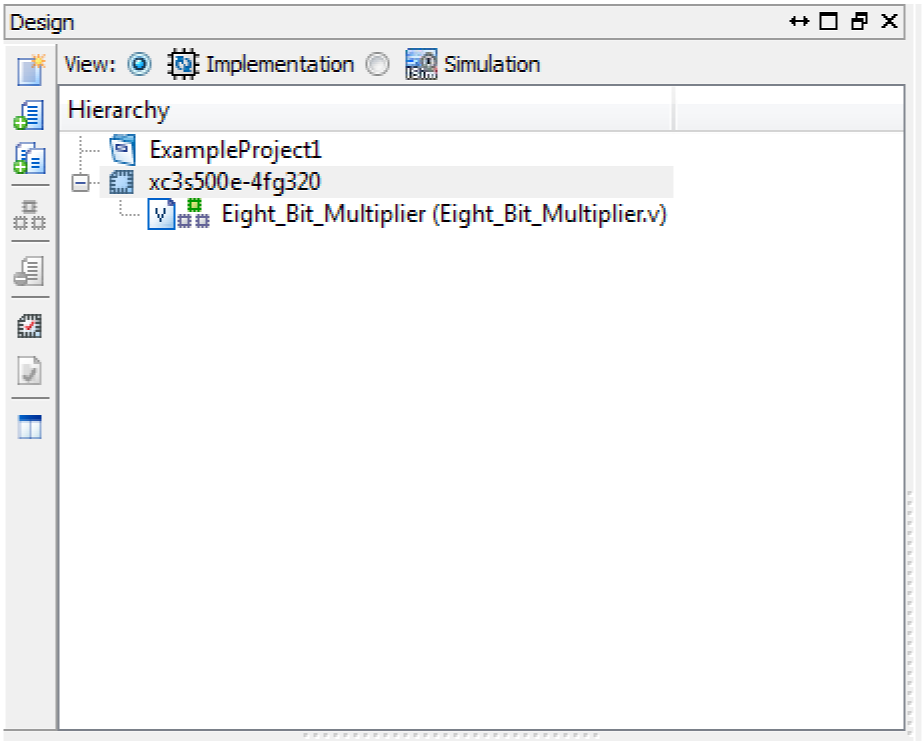
Project Navigator will create a new skeleton source with the following specifications.

Add to Project: Yes
Source Directory: D:\ExampleProject1
Source Type: Verilog Test Fixture
Source Name: Eight_Bit_Multiplier_tb.v

Association: Eight_Bit_Multiplier

a. Click Finish

b. Earlier in your Design Hierarchy in the top left of the ISE, you saw that your Verilog module was under the "Implementation" Section. This views your non-test fixtures.

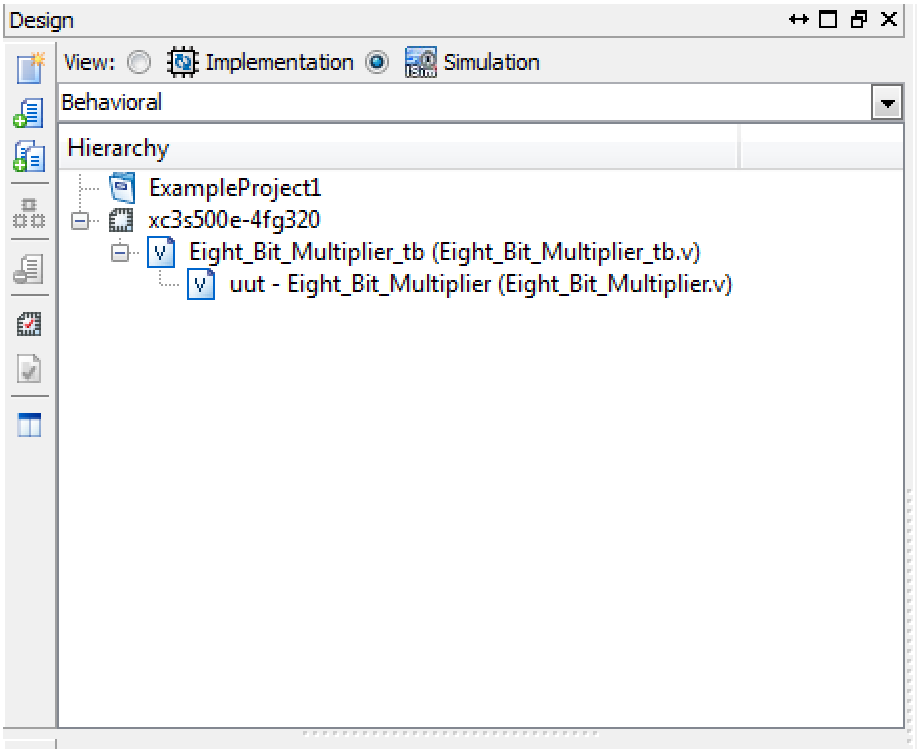


View: ● Implementation ○ Simulation

Hierarchy

- ExampleProject1
- xc3s500e-4fg320
  - Eight_Bit_Multiplier (Eight_Bit_Multiplier.v)

c. Click the "Simulation" circle to switch to view your projects simulations files



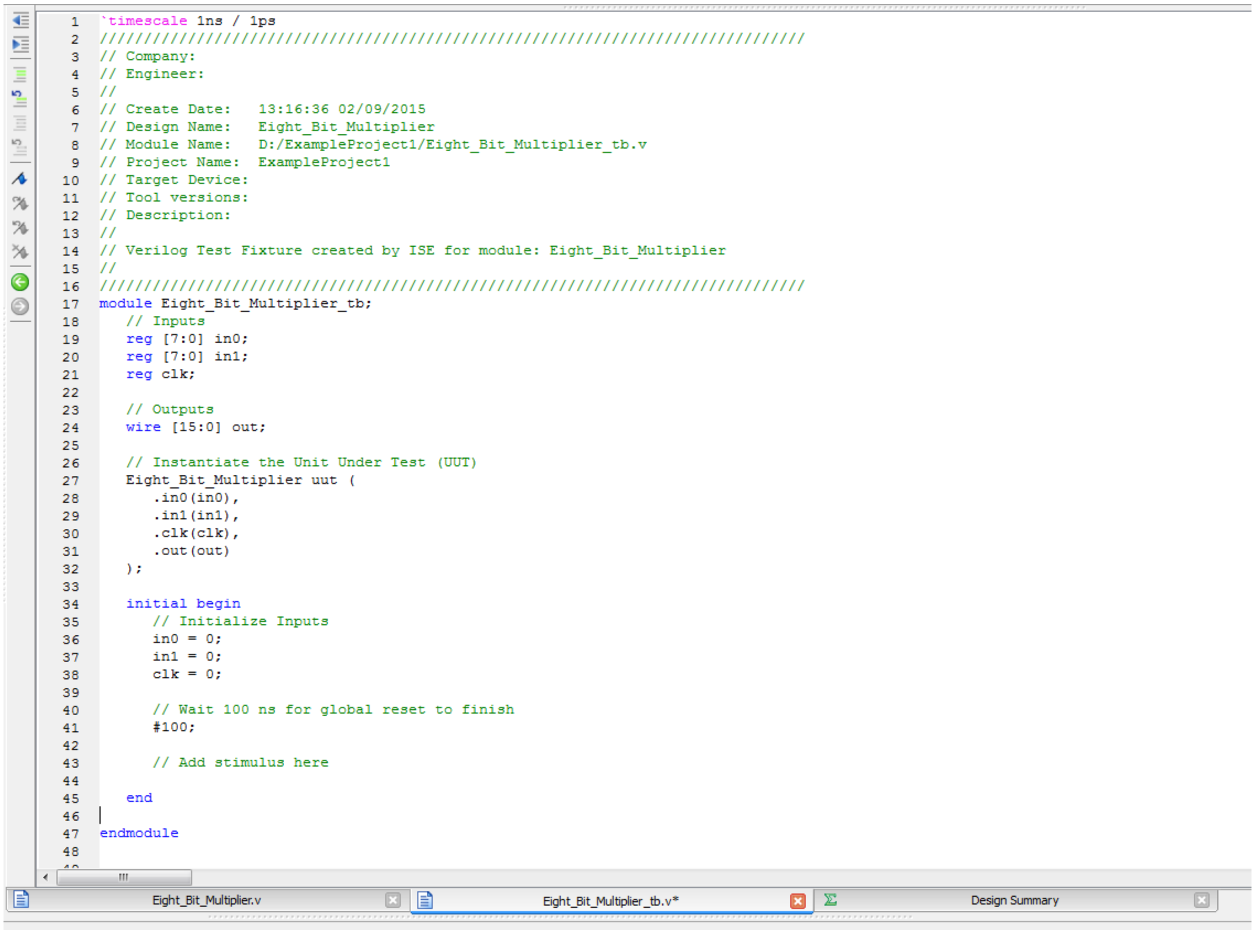
View: ○ Implementation ● Simulation

Behavioral

Hierarchy

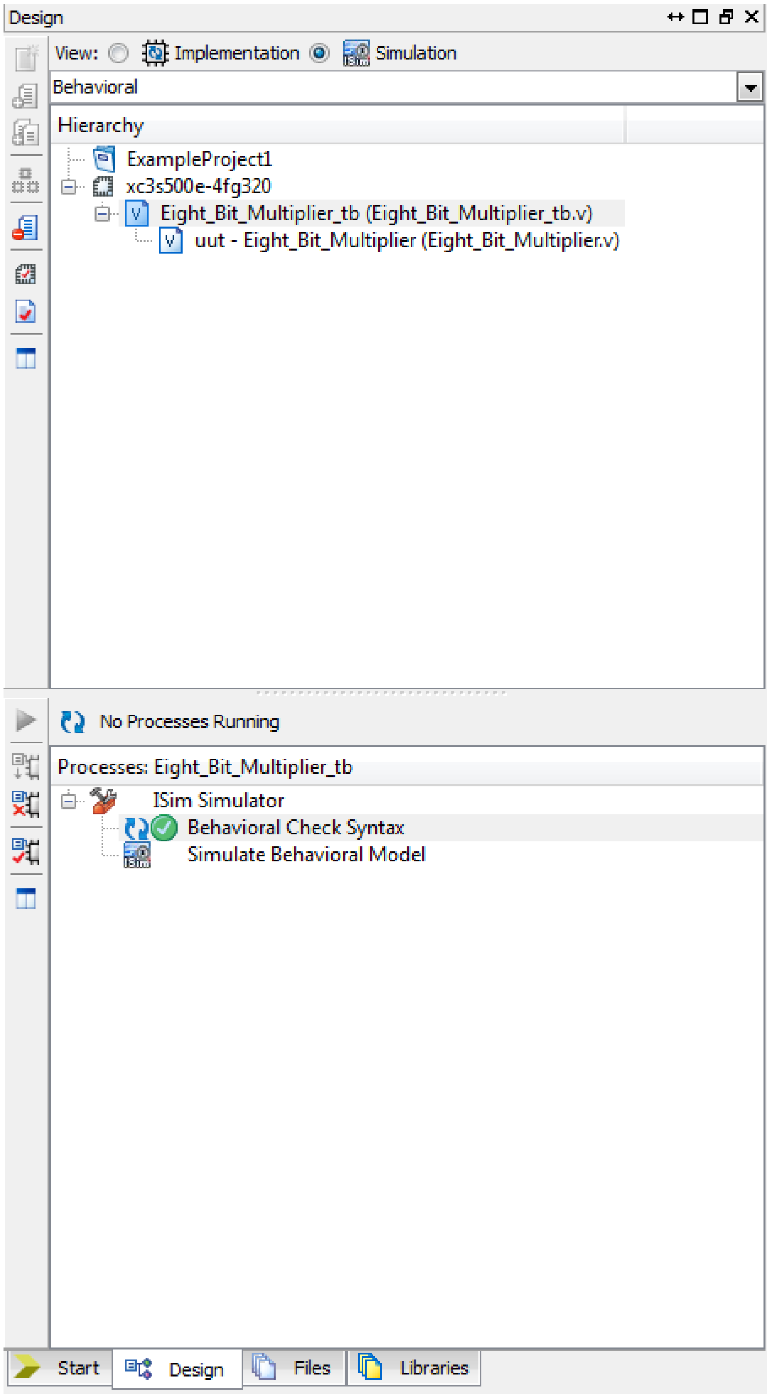
- ExampleProject1
- xc3s500e-4fg320
  - Eight_Bit_Multiplier_tb (Eight_Bit_Multiplier_tb.v)
    - uut - Eight_Bit_Multiplier (Eight_Bit_Multiplier.v)

d. This opens the file seen below. As you can see this testbench has auto generated inputs and outputs based on your Verilog module. It also creates an instantiation of the Verilog module that you are testing, in this case called “uut”, so you can test the module versus different inputs. It also initializes the inputs to the module you are testing.



```verilog
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   13:16:36 02/09/2015
// Design Name:   Eight_Bit_Multiplier
// Module Name:   D:/ExampleProject1/Eight_Bit_Multiplier_tb.v
// Project Name:  ExampleProject1
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: Eight_Bit_Multiplier
//
////////////////////////////////////////////////////////////////////////////////
module Eight_Bit_Multiplier_tb;
   // Inputs
   reg [7:0] in0;
   reg [7:0] in1;
   reg clk;

   // Outputs
   wire [15:0] out;

   // Instantiate the Unit Under Test (UUT)
   Eight_Bit_Multiplier uut (
      .in0(in0),
      .in1(in1),
      .clk(clk),
      .out(out)
   );

   initial begin
      // Initialize Inputs
      in0 = 0;
      in1 = 0;
      clk = 0;

      // Wait 100 ns for global reset to finish
      #100;

      // Add stimulus here

   end

endmodule

```

e. Make sure to run Behavioral Check Syntax to check your testbench code before simulating the behavioral model



ExampleProject1
xc3s500e-4fg320
Eight_Bit_Multiplier_tb (Eight_Bit_Multiplier_tb.v)
uut - Eight_Bit_Multiplier (Eight_Bit_Multiplier.v)

No Processes Running

Processes: Eight_Bit_Multiplier_tb
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model

13. Complete the Test Bench

a. Now it is time for you to write your own testbench, try this link for a tutorial about test benches and using ISim.

http://www.csee.umbc.edu/~tinoosh/cmpe415/tutorials/ISimTestbenchTutorial.pdf

b. A sample testbench file is listed here, provided by Dr. Tinoosh Mohsenin

http://www.csee.umbc.edu/~tinoosh/cmpe691/hw/HW1/tbench_template.v