Lab 1: Tools tutorial
CMPE 415
UMBC

February 1st, 2012
Due February 8th 2012 (at 2:30 pm)

1 Objective

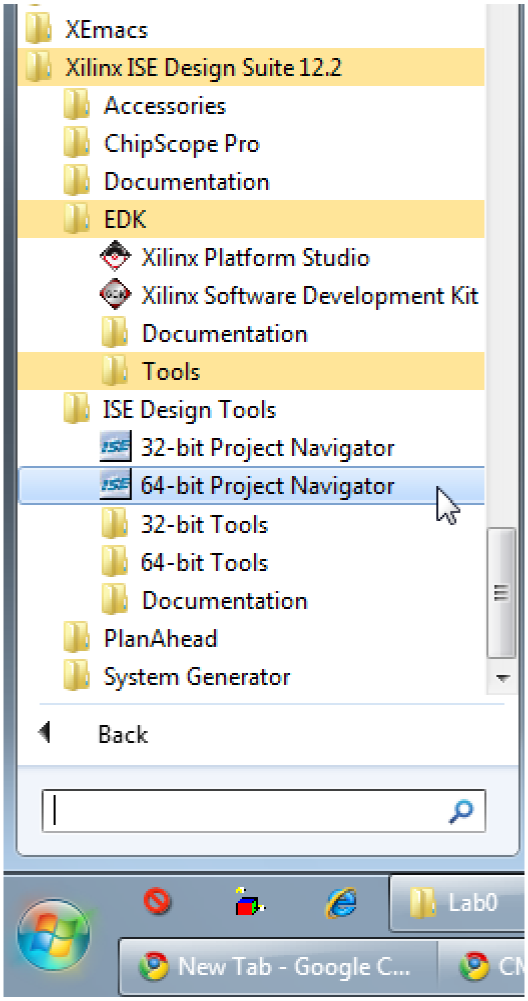
The objective of this lab is to learn the fundamental components of the Xilinx FGPA tools required to enter and assemble HDL code using a schematic entry tool and program an FPGA. This includes integrating HDL into a schematic, as well as creating and updating symbols.

2 Intro

In this lab you will program an FPGA to display a rectangle on a monitor using a VGA cable. You will _rst create an implementation with an error in it and view the results. You will then modify the code, update the symbol in the schematic, and wire the schematic correctly to control the color of the rectangle using switches.

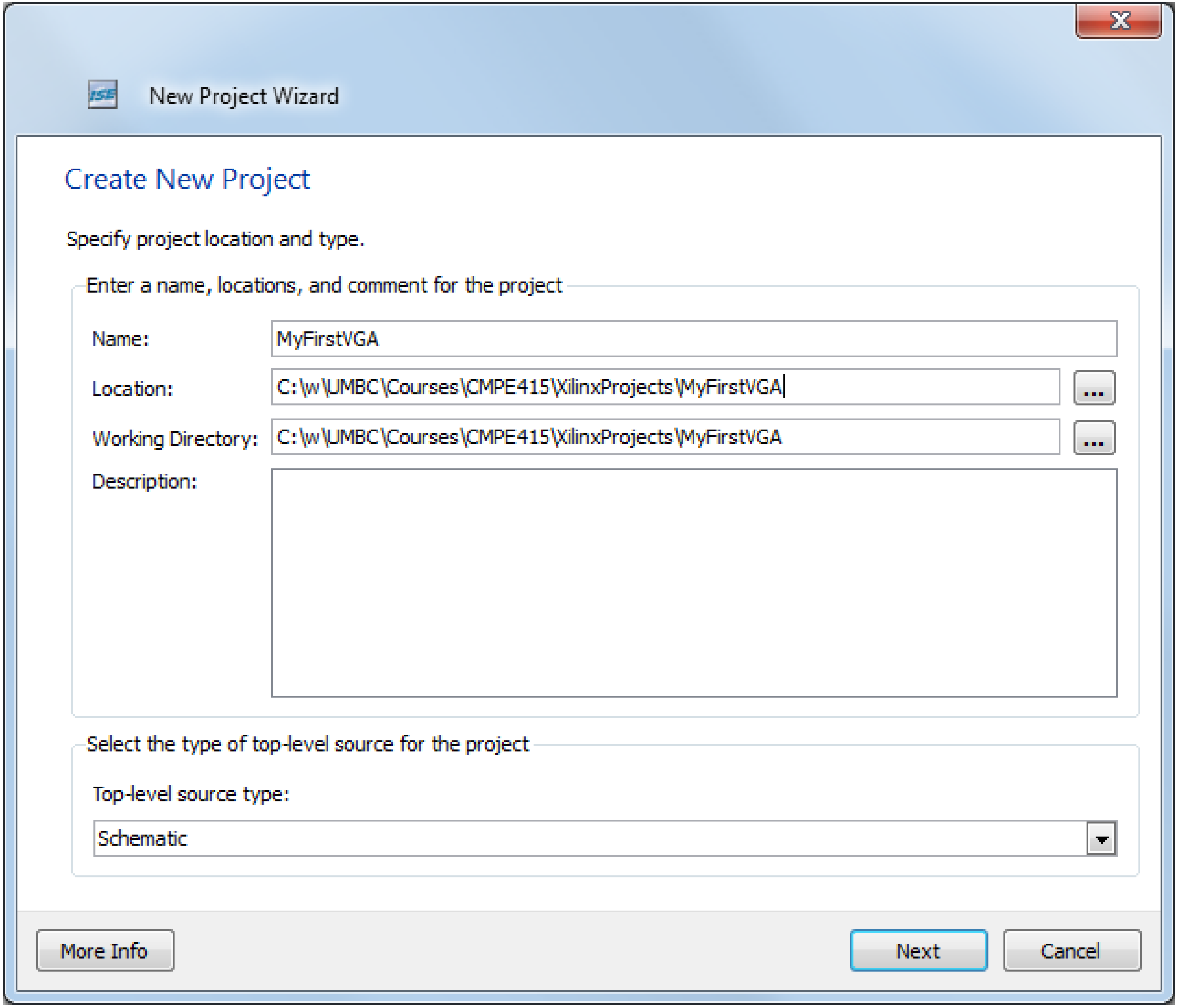
3 Tutorial Steps

3.1 Start Xlinx Tool



3.2 Create New Project

1. In main window menu: File->New Project...



New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: MyFirstVGA

Location: C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

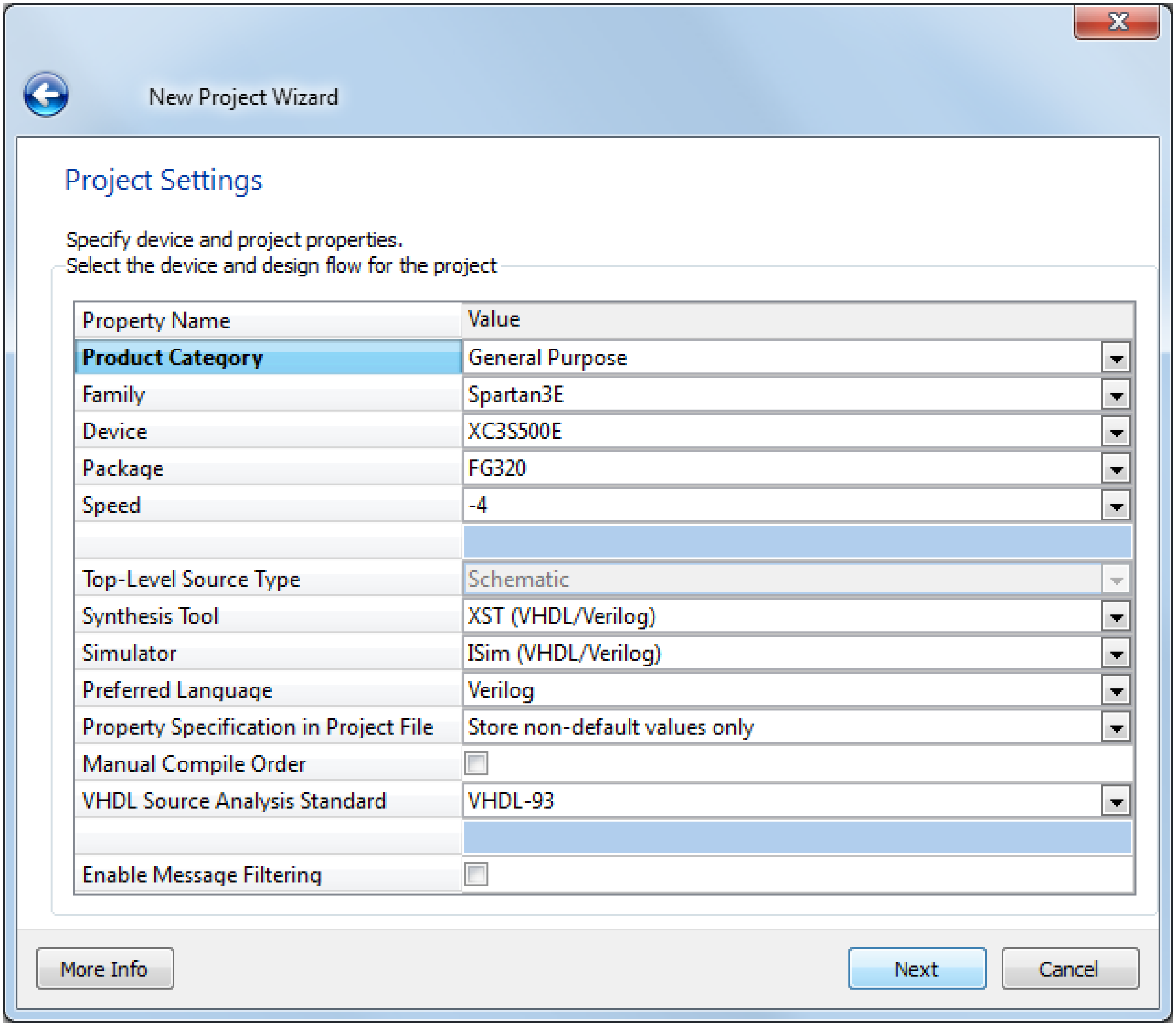
Working Directory: C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

Description:

Select the type of top-level source for the project

Top-level source type: Schematic

2. You'll now need to enter information about the FPGA. You can look in "Spartan-3E FPGA Family: Data Sheet" under Package Marking (page 6). To find this information. http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf



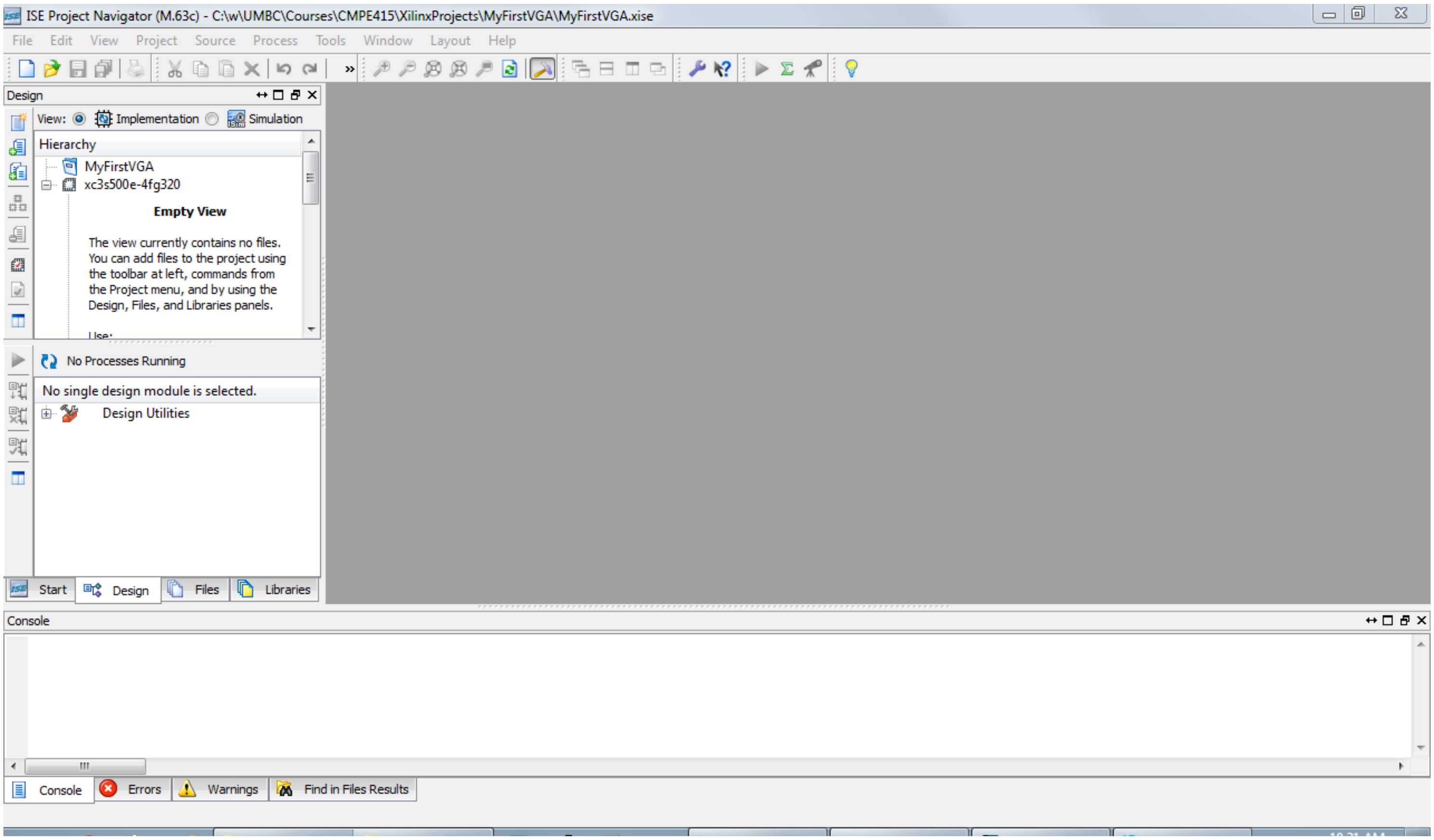
Project Settings

Specify device and project properties.

Select the device and design flow for the project

Property Name	Value
Product Category	General Purpose
Family	Spartan3E
Device	XC3S500E
Package	FG320
Speed	-4
Top-Level Source Type	Schematic
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store non-default values only
Manual Compile Order	☐
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	☐

3. The next screen shows a summay. Hit Finish. Result:



Empty View

The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.

Use:

No single design module is selected.

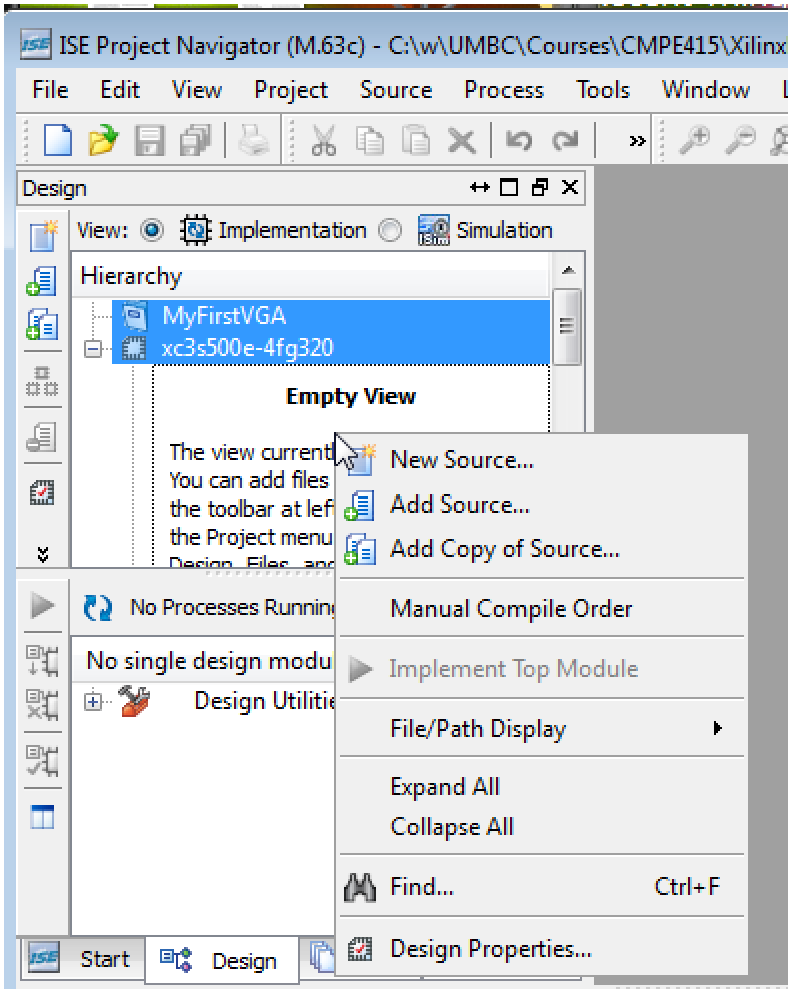
3.3 Downloaded HDL Module and Add to project

1. Download a free HDL description of implementation of a vga module to a temporary directory or to your project directory. Our other module will be implmented using Verilog, but we can integrate Verilog and VHDL modules together in the schematic if desired. Here are examples of the type of vga modules for which you are looking. Make sure to respect any restrictions the authors place on copywrighted code that you use.

   - ***http://web.mit.edu/6.111/www/f2005/code/jtag2mem_6111/vga_sync.v Verilog implementation (I suggest this one.)***
   - http://www.ece.gatech.edu/academic/courses/fpga/Xilinx/downloads/vga_sync.vhd VHDL implementation (handles blanking internally)
   - http://jjackson.eng.ua.edu/courses/ece480/assignments/vga_sync.vhd VHDL implementation with parameters to set various resolutions (also, implements a "video_on" signal instead of a "blank" signal)

2. There are three places to access the project functions, such as adding a source. You can use any of the following (a,b,c):

   (a) Right-click in the Hierarchy plane



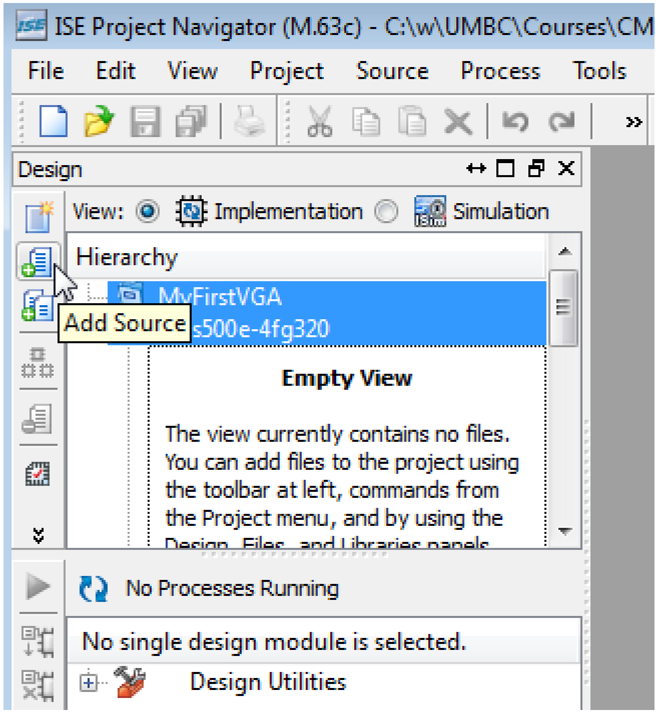
Empty View

The view current
You can add files
the toolbar at lef
the Project menu
Design, Files, and

No Processes Runnin

No single design modu

(b) Use the buttons along the left.



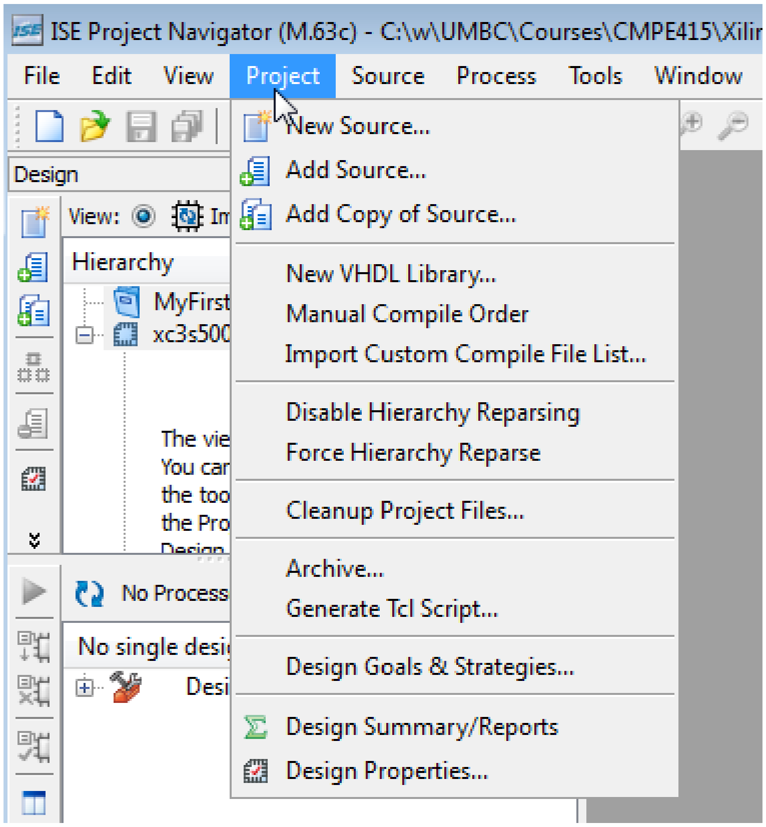
Empty View

The view currently contains no files. You can add files to the project using the toolbar at left, commands from the Project menu, and by using the Design, Files, and Libraries panels.

No Processes Running

No single design module is selected.

(c) Use the main window Project menu



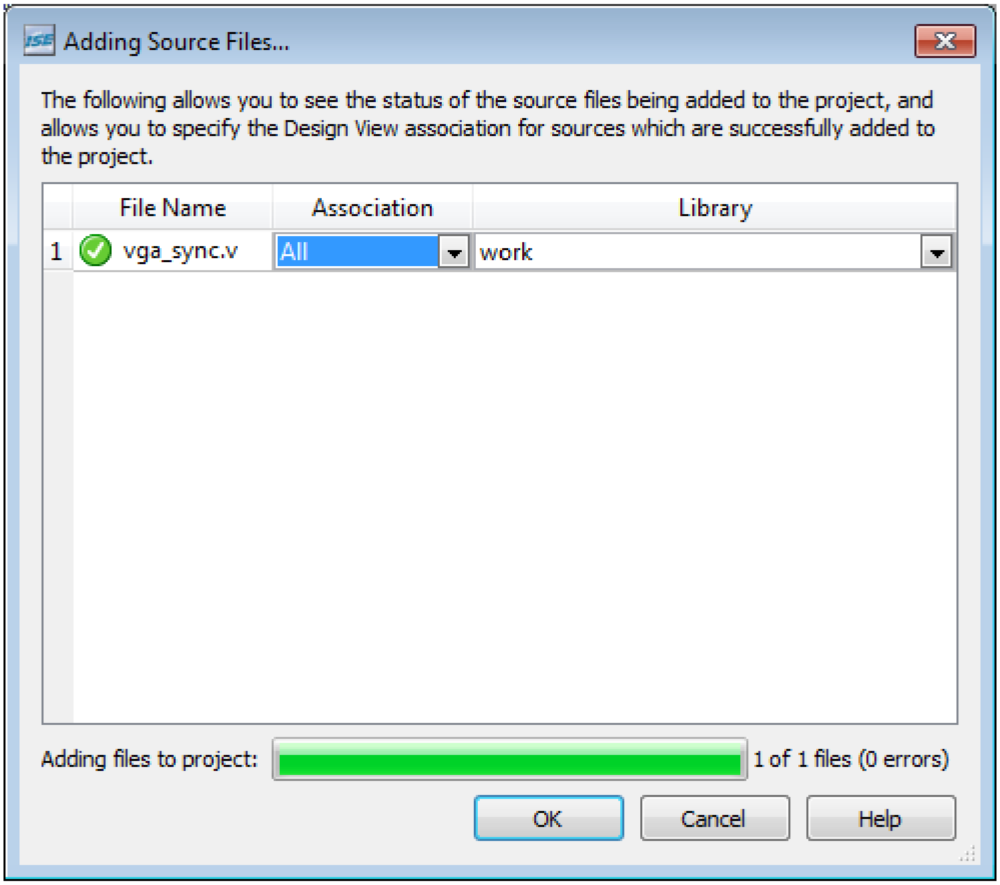
3. The three functions for sources are:

   (a) New Source - starts wizard to create a new source file (Verilog, VHDL, Schematic, etc...), creating a shell if desired, and adds it for use in the project.

   (b) Add Source - Allows you to point to a source file in the project directory or anywhere else and include it for use in the project

   (c) Add Copy of Source - Creates a copy of the source file in the project directory and adds the copy for use in the project

   - Add the downloaded HDL file using option (b) “Add Source” if you initially downloaded the file to project directory and use option (c) “Add Copy of Source” if you downloaded it to a temporary directory.

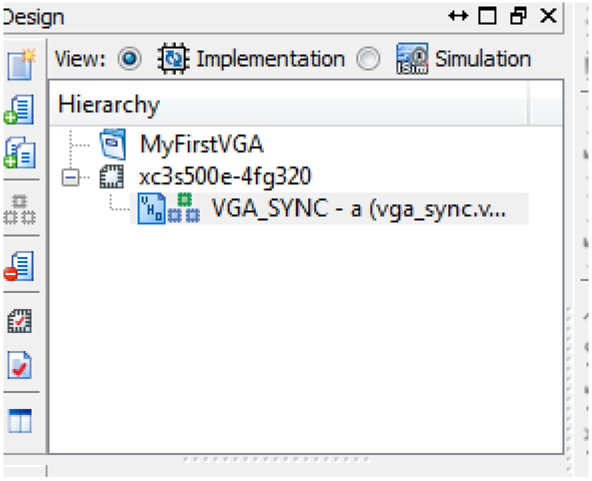


The following allows you to see the status of the source files being added to the project, and allows you to specify the Design View association for sources which are successfully added to the project.

	File Name	Association	Library
1	✓ vga_sync.v	All	work

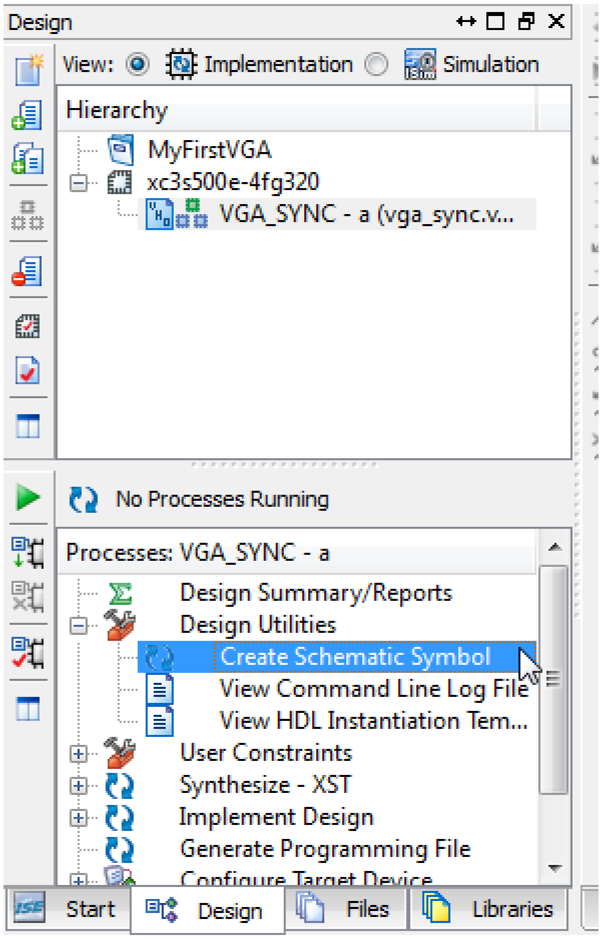
Adding files to project: 1 of 1 files (0 errors)

- You will now have a new source listed.


Design
View: ● Implementation ○ Simulation
Hierarchy
MyFirstVGA
xc3s500e-4fg320
VGA_SYNC - a (vga_sync.v...

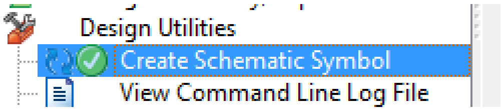
3.4 Creating a Symbol

1. Select the new HDL source in the Hierarchy panel. In the lower panel expand Design Utilities and double-click “Create Schematic Symbol”.



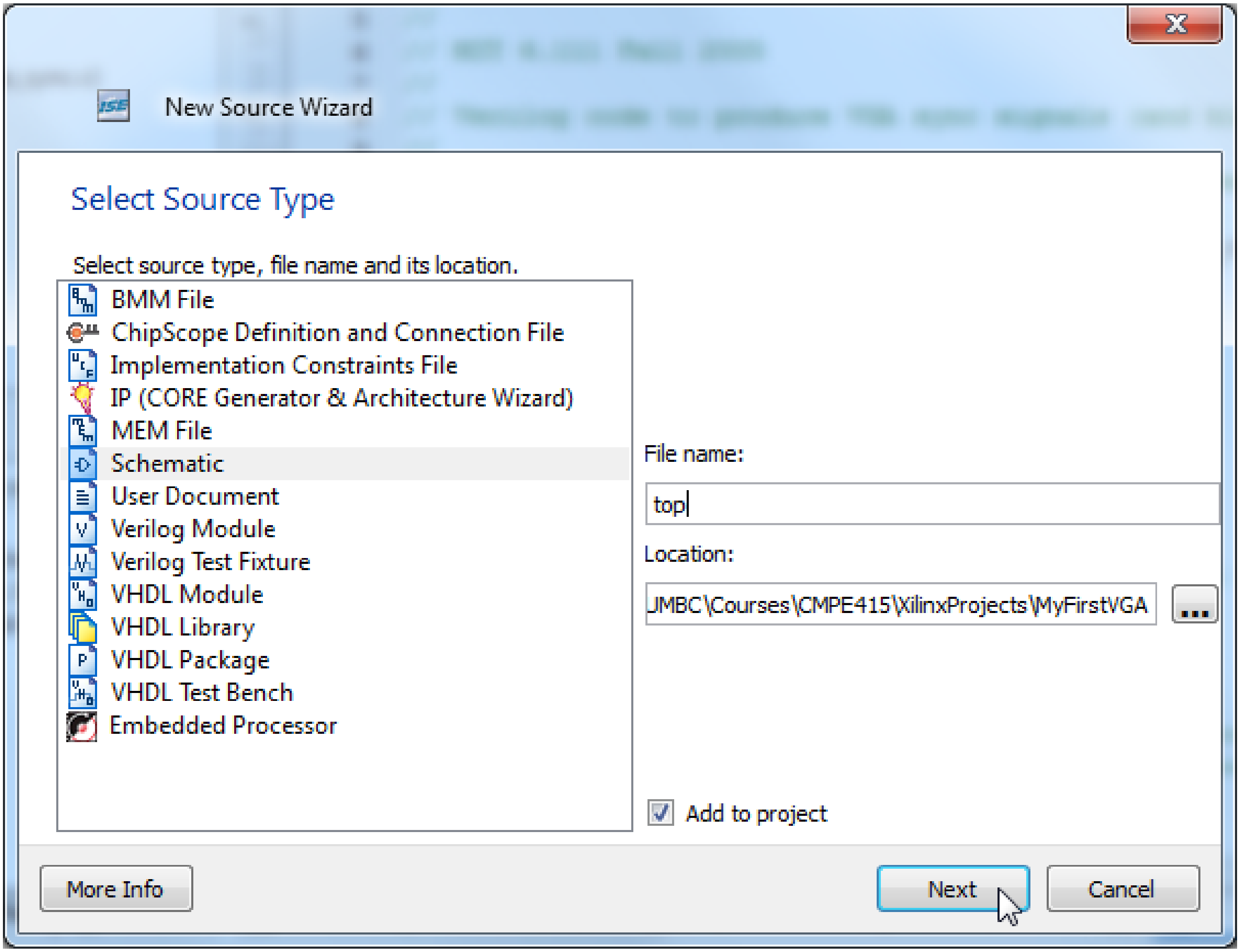
If needed, see help of: Creating a Schematic Symbol from a Source File Help->Help Topics

2. Notice the green check mark added upon success.



3.5 Create Top Schematic

1. Using the main window Project menu, the buttons along the left, or a right-click in the Hierarchy view create a new source.
2. Project->New Source...
3. The New Source Wizard opens
4. Select Schematic as the type and top as the File Name. Click Next.



New Source Wizard

Select Source Type

Select source type, file name and its location.

Schematic

File name: top

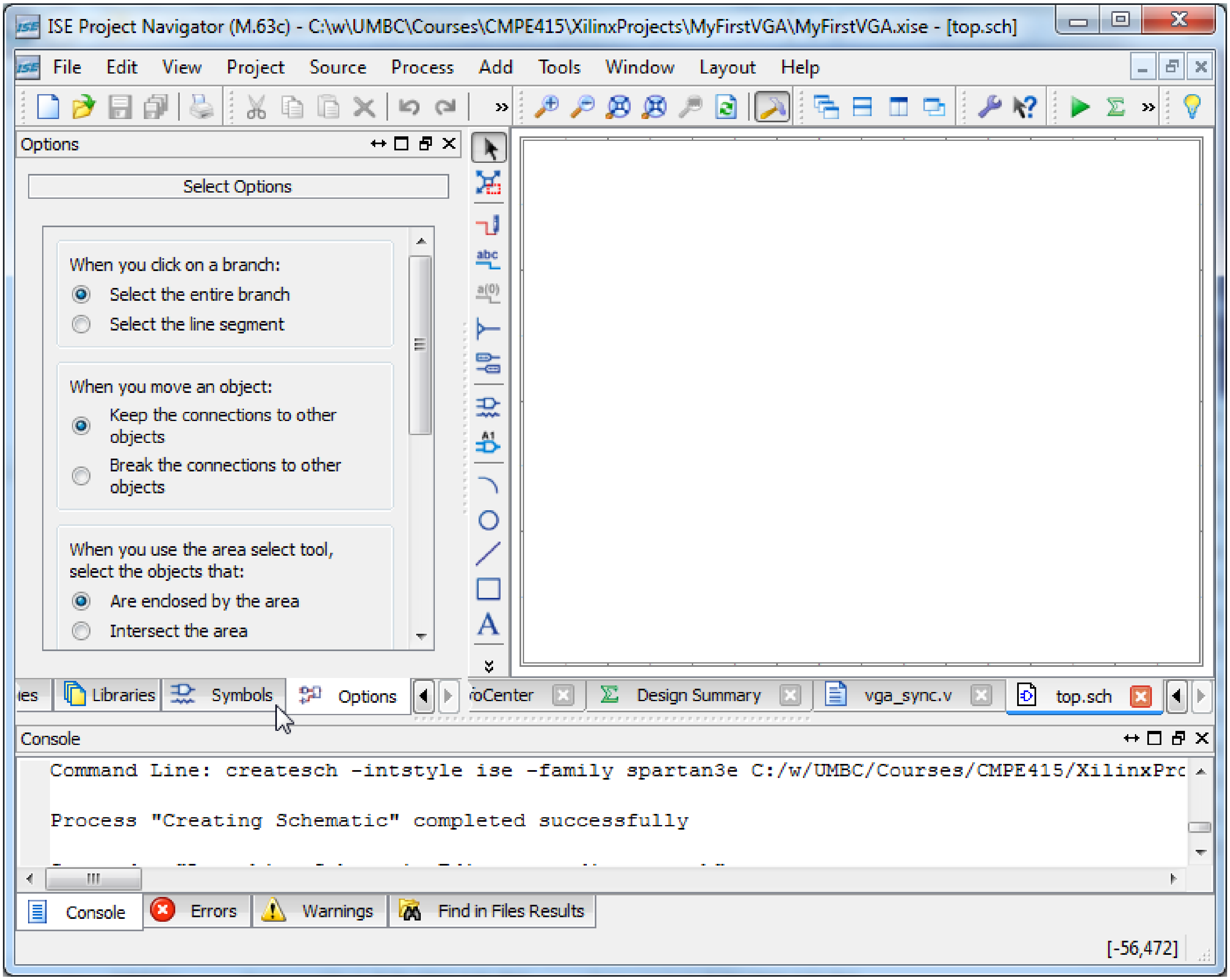
Location: JMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

☑ Add to project

5. Click Finish in the following window.

3.6 Add Symbol

1. With your fresh sechmaic showing, select the Symbols tab as pointed out by the cursor in the picture. (use the scroll buttons just to the right if not shown)



When you click on a branch:

● Select the entire branch

○ Select the line segment

When you move an object:

● Keep the connections to other objects

○ Break the connections to other objects

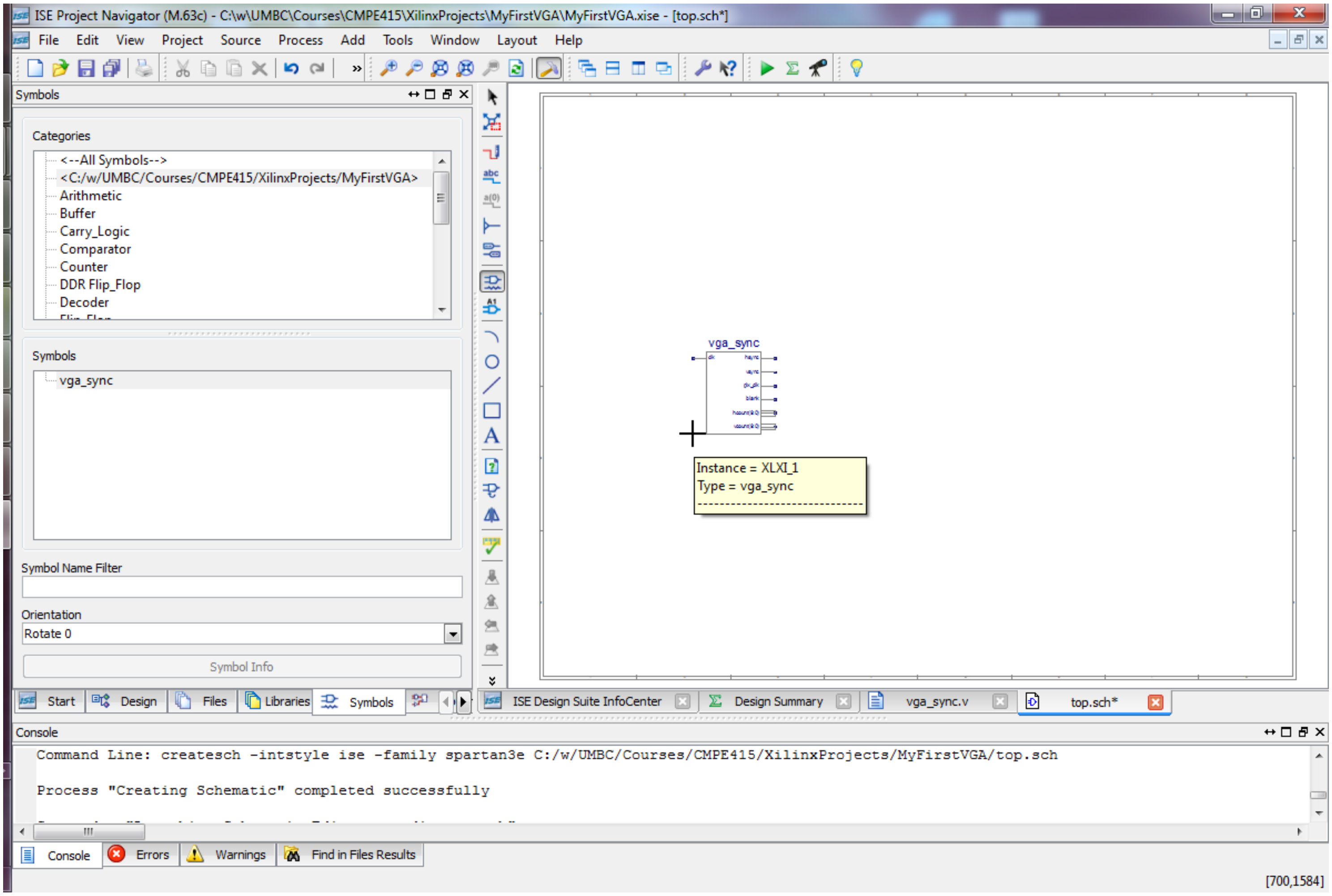
When you use the area select tool, select the objects that:

● Are enclosed by the area

○ Intersect the area

```
Command Line: createsch -intstyle ise -family spartan3e C:/w/UMBC/Courses/CMPE415/XilinxPro

Process "Creating Schematic" completed successfully
```

2. Under Catagories, select your current project.
3. Under symbols, select your new symbol
4. Click in the schematic to add the symbol.



ISE Project Navigator (M.63c) - C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA\MyFirstVGA.xise - [top.sch*]

Categories:
- <--All Symbols-->
- <C:/w/UMBC/Courses/CMPE415/XilinxProjects/MyFirstVGA>
- Arithmetic
- Buffer
- Carry_Logic
- Comparator
- Counter
- DDR Flip_Flop
- Decoder

Symbols: vga_sync

Symbol Name Filter:

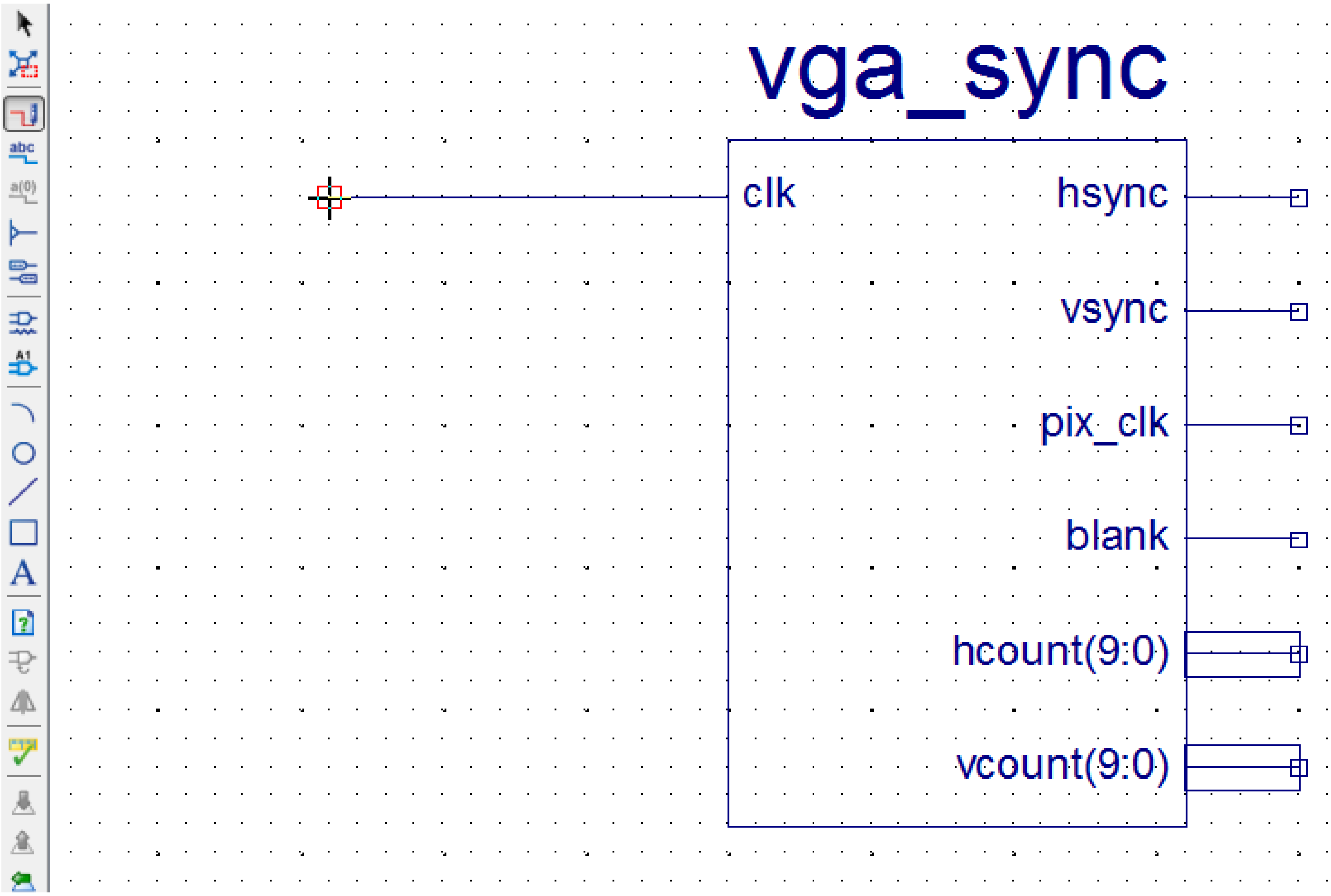
Orientation: Rotate 0

Instance = XLXI_1
Type = vga_sync

```
Command Line: createsch -intstyle ise -family spartan3e C:/w/UMBC/Courses/CMPE415/XilinxProjects/MyFirstVGA/top.sch

Process "Creating Schematic" completed successfully
```

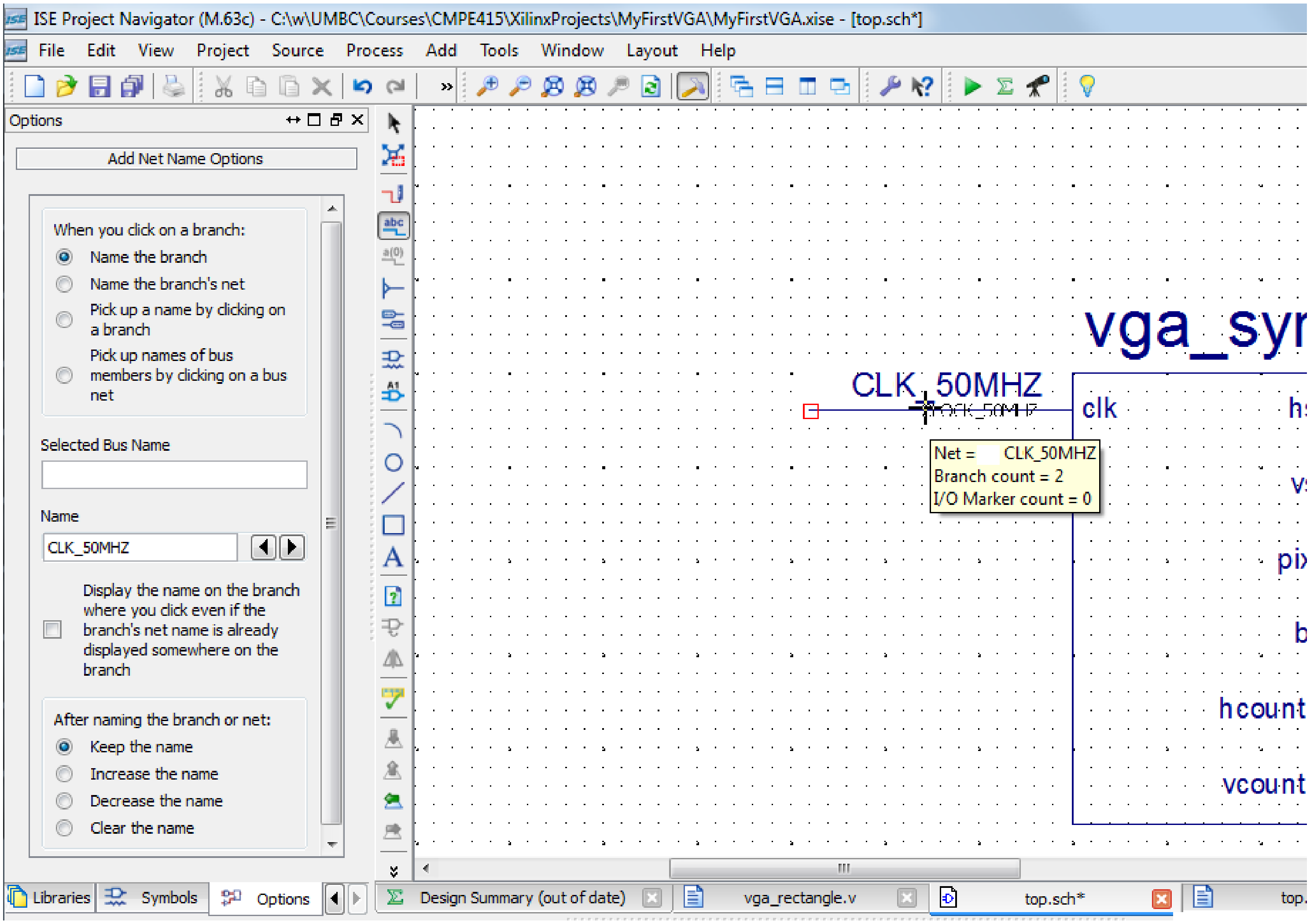
3.7 Add wire, name it, and and pin

1. Using Add menu or other documented means, choose Add->Wire
2. Click twice to add a simple wire as shown.



3. Add->Net Name

4. Type Name CLK_50MHZ, and click on wire



ISE Project Navigator (M.63c) - C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA\MyFirstVGA.xise - [top.sch*]

Options

Add Net Name Options

When you click on a branch:

● Name the branch
○ Name the branch's net
○ Pick up a name by clicking on a branch
○ Pick up names of bus members by clicking on a bus net

Selected Bus Name

Name: CLK_50MHZ

□ Display the name on the branch where you click even if the branch's net name is already displayed somewhere on the branch

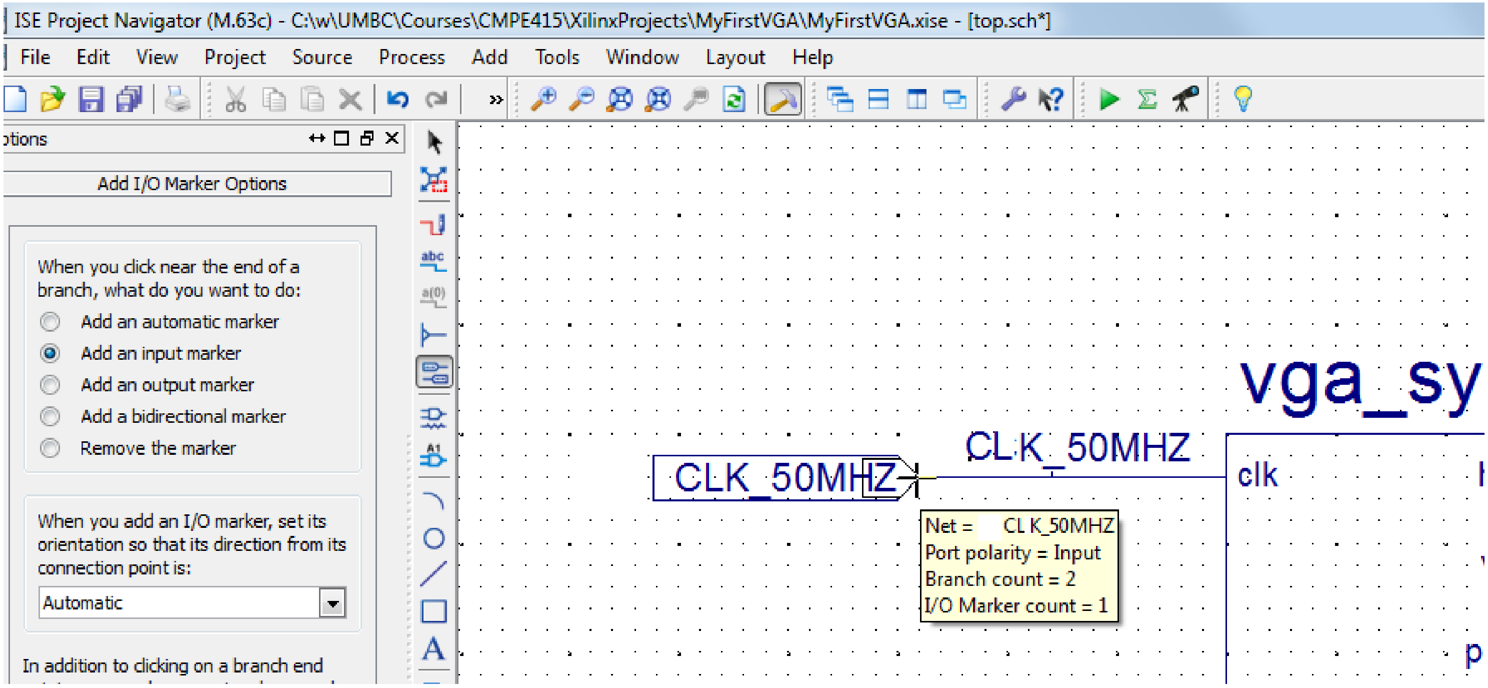
After naming the branch or net:

● Keep the name
○ Increase the name
○ Decrease the name
○ Clear the name

Net = CLK_50MHZ
Branch count = 2
I/O Marker count = 0

5. Next, add pin (I/O Marker): Use Menu Add->I/O Marker

6. Select "Add an input marker" on left and click on end of wire.



ISE Project Navigator (M.63c) - C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA\MyFirstVGA.xise - [top.sch*]

ptions

Add I/O Marker Options

When you click near the end of a branch, what do you want to do:

○ Add an automatic marker
● Add an input marker
○ Add an output marker
○ Add a bidirectional marker
○ Remove the marker

When you add an I/O marker, set its orientation so that its direction from its connection point is:

Automatic

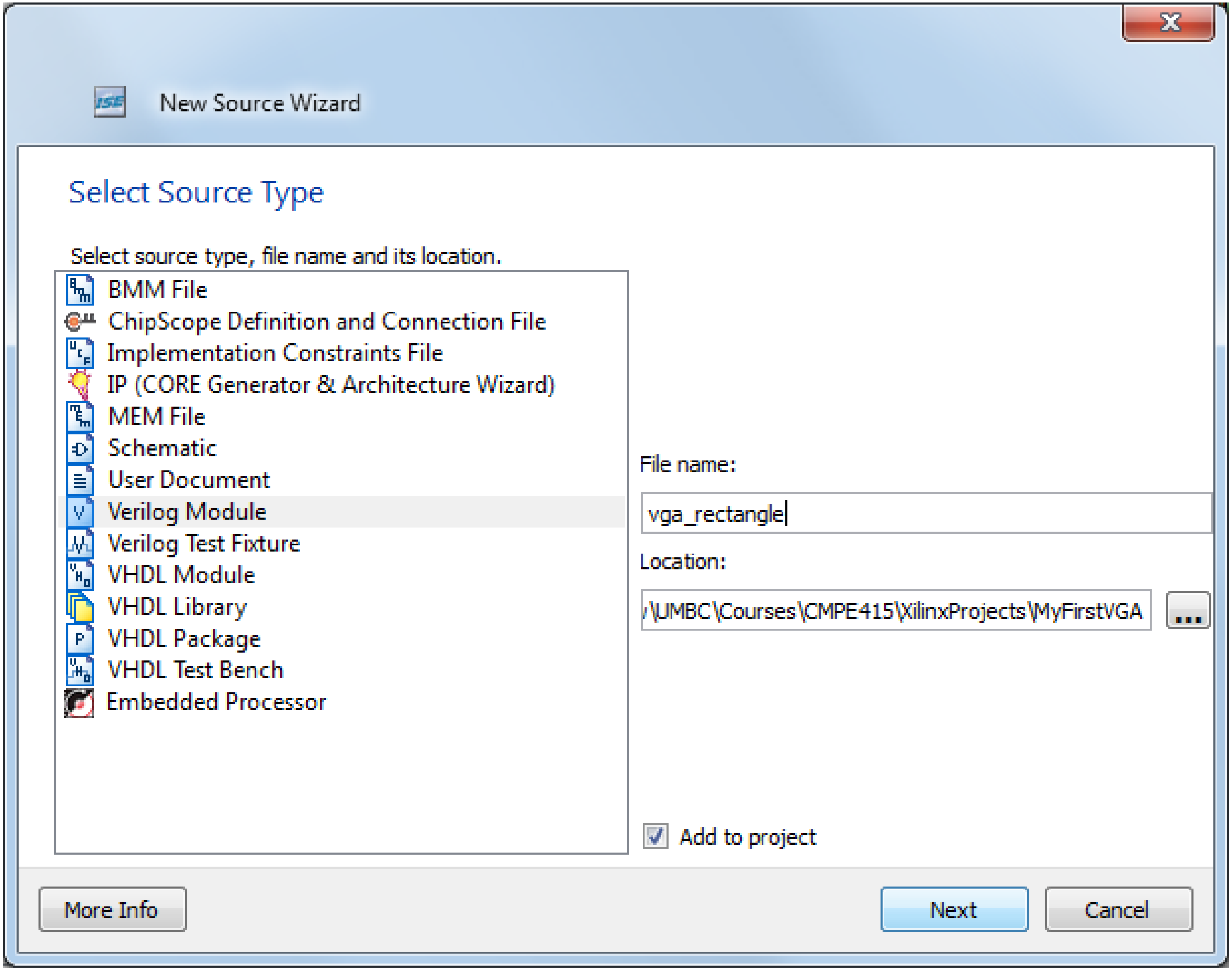
In addition to clicking on a branch end

Net = CLK_50MHZ
Port polarity = Input
Branch count = 2
I/O Marker count = 1

3.8 Add New Source for rectangle display driver using Source Wizard

1. Main window menu: Project->New Source

2. Select Verilog Module, enter File name vga_rectangle, click Next



New Source Wizard

Select Source Type

Select source type, file name and its location.

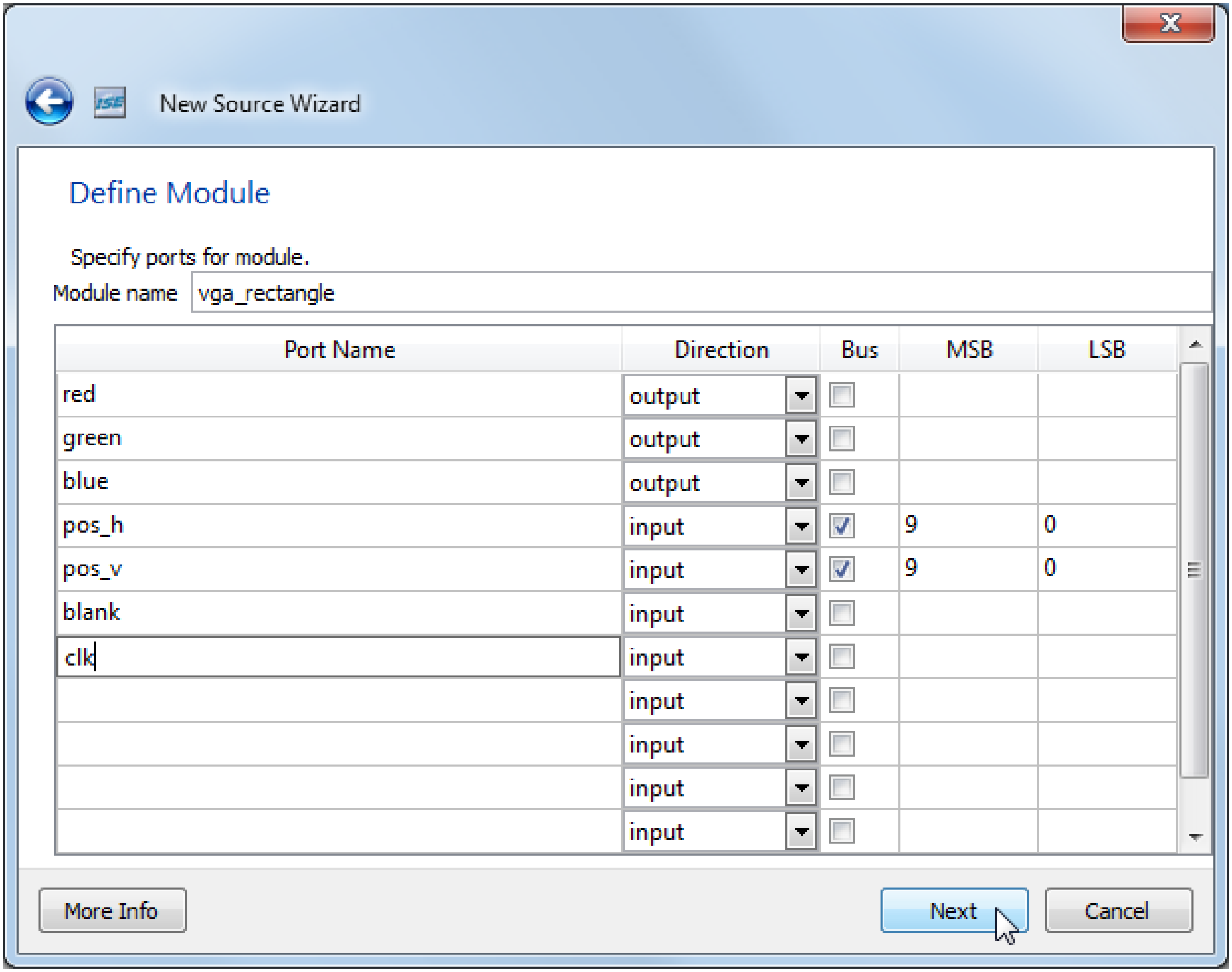
- BMM File
- ChipScope Definition and Connection File
- Implementation Constraints File
- IP (CORE Generator & Architecture Wizard)
- MEM File
- Schematic
- User Document
- Verilog Module
- Verilog Test Fixture
- VHDL Module
- VHDL Library
- VHDL Package
- VHDL Test Bench
- Embedded Processor

File name: vga_rectangle

Location: \UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

☑ Add to project

3. Set up the IO as shown and then click Next and then click Finish in the following window.



Define Module

Specify ports for module.

Module name: vga_rectangle

Port Name	Direction	Bus	MSB	LSB
red	output	☐		
green	output	☐		
blue	output	☐		
pos_h	input	☑	9	0
pos_v	input	☑	9	0
blank	input	☐		
clk	input	☐		
	input	☐		
	input	☐		
	input	☐		
	input	☐		

4. You should now have a shell created with port definitions. Set the reg, green, and blue outputs as registers. Implementing registers avoids glitching (not that it is critical here).
   change

   ```
   output red,
   output green,
   output blue,
   ```

   to

   ```
   output reg red,
   output reg green,
   output reg blue,
   ```

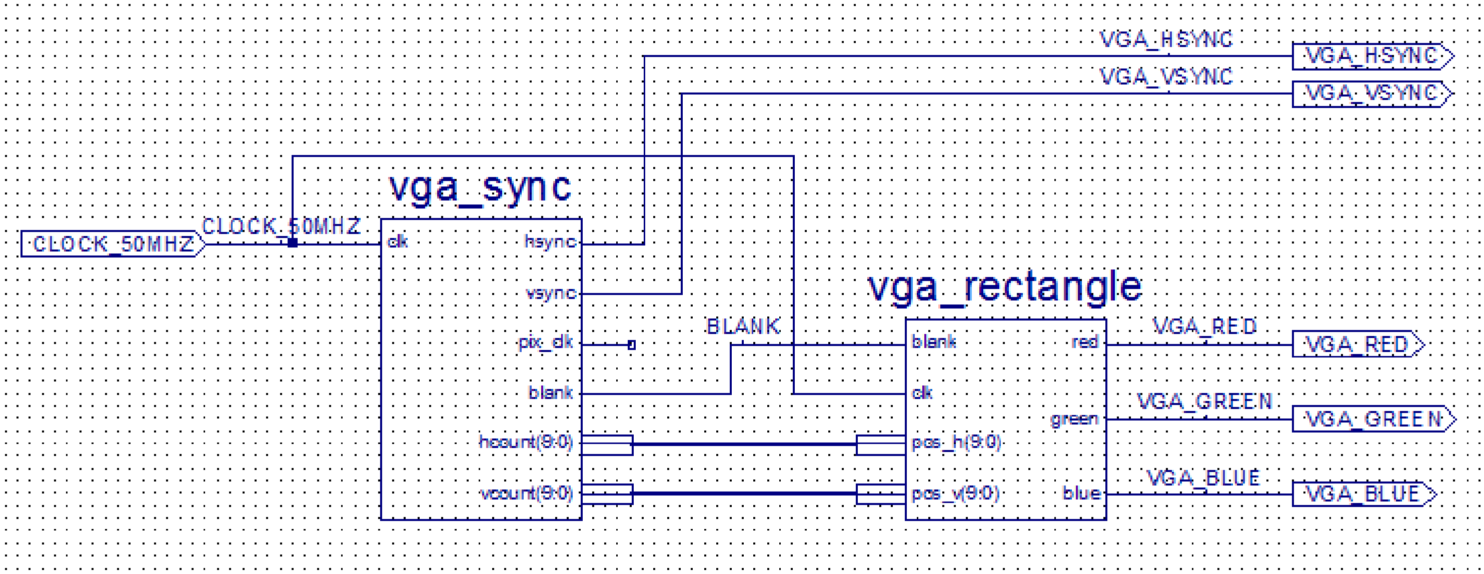
5. Add the following module code:

```
 parameter WIDTH    =  20;
 parameter HIEGHT   = 100;
 parameter X_LEFT   = 320;
 parameter Y_BOTTOM = 240;

 //addinal intermediate logic signal wires
 wire flag_on_rect;   //high only when over rectangle
 wire [9:0] x,y;      //traditional cartesean coordinates, (left, bottom)=(0,0)

 //combinatorial logic to calculate x,y coordinate system
 assign x = pos_h;
 assign y = 480 - pos_v;

 //combinatorial logic to decide if beam is over a rectange
 assign flag_on_rect = x >= (X_LEFT)           &&
                       x <  (X_LEFT + WIDTH)   &&
                       y >= (Y_BOTTOM)         &&
                       y <  (Y_BOTTOM + HIEGHT);

//combinatorial logic and registers that load on rising clock edge
always @(posedge clk) begin
         red   <=  flag_on_rect & ~blank;
         green <= ~flag_on_rect & ~blank;
     blue  <=  flag_on_rect & ~blank;
 end
```

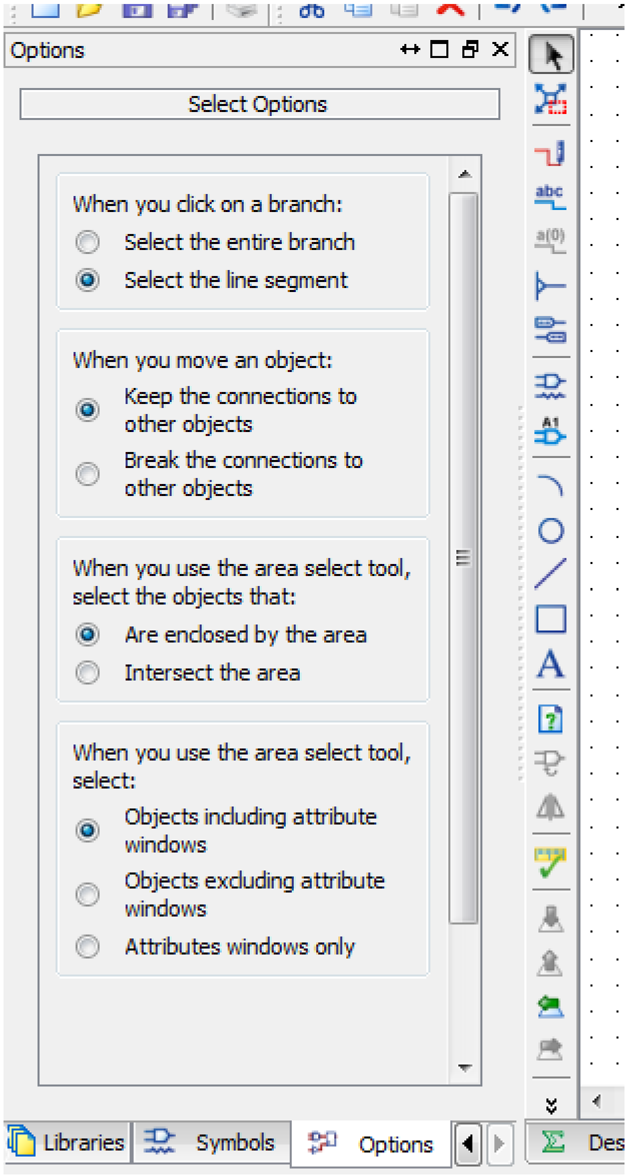
6. Save the file and generate a symbol as before

3.9 Complete Top Schematic

1. Complete the schematic as follows, including the output markers (be sure to make them as output markers, not input markers)



- Note the IMPORTANT OPTIONS for the Select(Arrow) tool. Thouroghly understand the first three options, reading the documentation as nessisary. Understanding these options could save you a lot of time.



When you click on a branch:
○ Select the entire branch
● Select the line segment

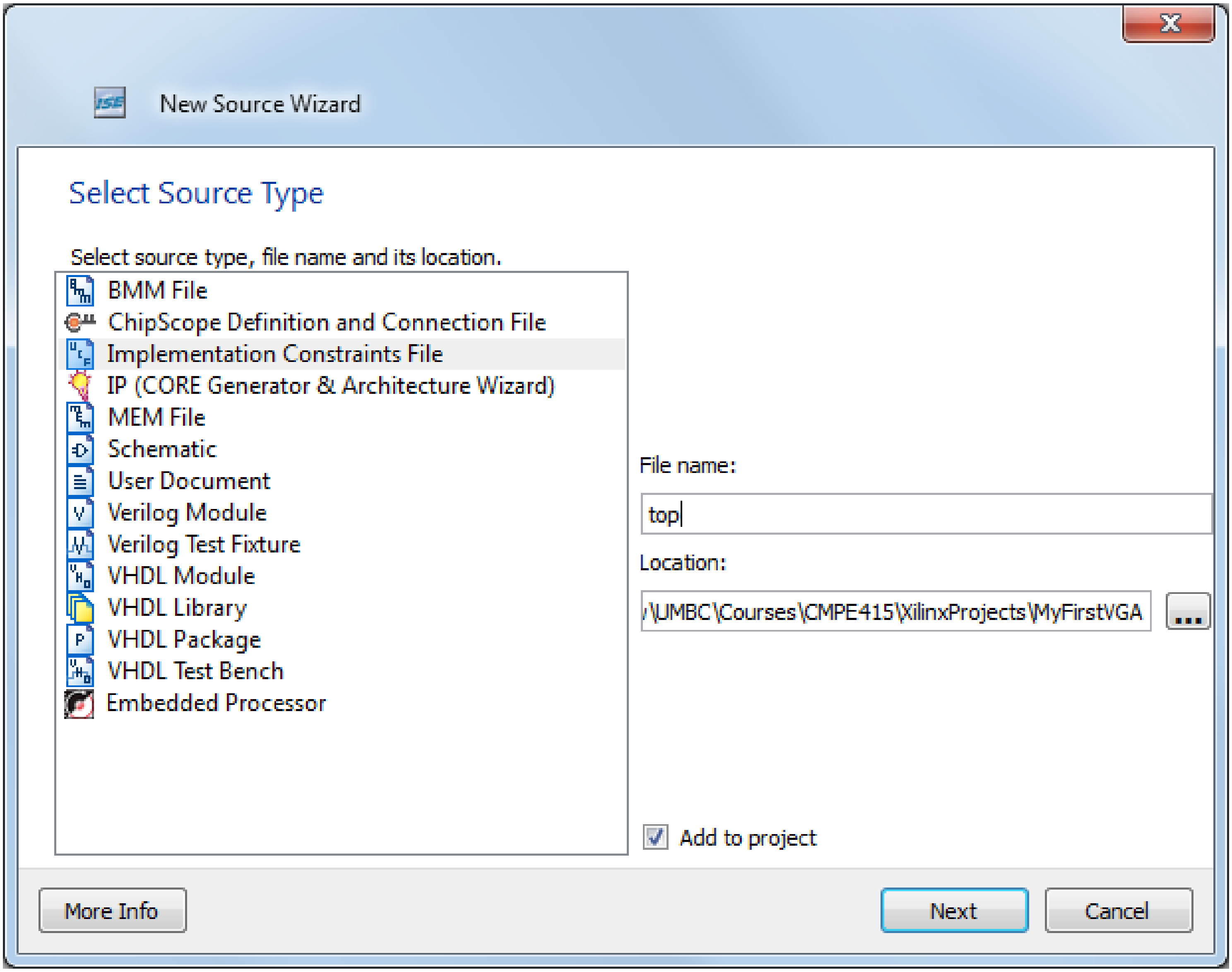
When you move an object:
● Keep the connections to other objects
○ Break the connections to other objects

When you use the area select tool, select the objects that:
● Are enclosed by the area
○ Intersect the area

When you use the area select tool, select:
● Objects including attribute windows
○ Objects excluding attribute windows
○ Attributes windows only

3.10 Define Pin Locations

1. We need to add a user contrainst file. Use the new source wizard or create one called top: Project->New Source...



File name: top

Location: \UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

☑ Add to project

2. Click Next then Finish.

   Page 57 of the developement board user guide provides pin locations for the vga port: http://www.digilentinc.com/Data/Pro

   Appendix B provides an Example User Constraints File (UCF) for the starter board, starting on page 159.

3. Copy the following lines to your UCF:

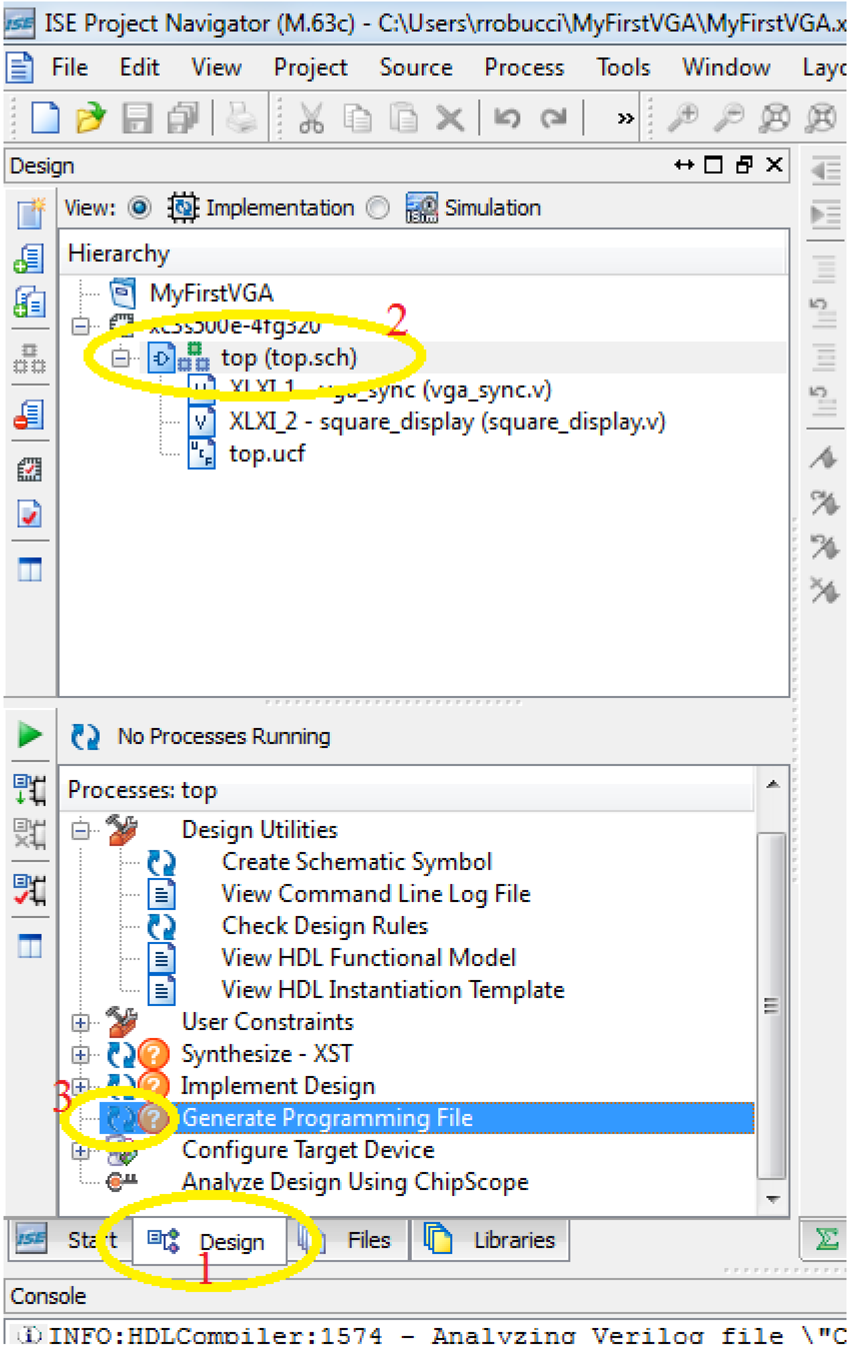
```
# ==== Clock inputs (CLK) ====
NET "CLK_50MHZ" LOC = "C9"  | IOSTANDARD = LVCMOS33 ;
#       Define clock period for 50 MHz oscillator (40%/60% duty-cycle)
NET "CLK_50MHZ" PERIOD = 20.0ns HIGH 40%;
# ==== VGA Port (VGA) ====
NET "VGA_BLUE"   LOC = "G15" | IOSTANDARD = LVTTL  | DRIVE = 8  | SLEW = FAST ;
NET "VGA_GREEN"  LOC = "H15" | IOSTANDARD = LVTTL  | DRIVE = 8  | SLEW = FAST ;
NET "VGA_HSYNC"  LOC = "F15" | IOSTANDARD = LVTTL  | DRIVE = 8  | SLEW = FAST ;
NET "VGA_RED"    LOC = "H14" | IOSTANDARD = LVTTL  | DRIVE = 8  | SLEW = FAST ;
NET "VGA_VSYNC"  LOC = "F14" | IOSTANDARD = LVTTL  | DRIVE = 8  | SLEW = FAST ;
```

3.11 Synthesize, Implement, and Generate Programmaing File

1. On the left, bring up the design view by clicking the design tab
2. Then in the Hierarchy plan, select the top module in the design, top.sch

3. Finallly, DOUBLE-CLICK Generate Programming File in the plane below.

    - “Synthesize” and “Implement Design” are run automatically as needed.
        - Sythesize maps your design to a circuit based on FPGA build blocks.
        - Implement Design maps the circuit to the FPGA including place and route.


ISE Project Navigator (M.63c) - C:\Users\rrobucci\MyFirstVGA\MyFirstVGA.x
File
Edit
View
Project
Source
Process
Tools
Window
Layo
Design
View: ● Implementation ○ Simulation
Hierarchy
MyFirstVGA
xc3s500e-4fg320
top (top.sch)
XLXI_1 - vga_sync (vga_sync.v)
XLXI_2 - square_display (square_display.v)
top.ucf
No Processes Running
Processes: top
Design Utilities
Create Schematic Symbol
View Command Line Log File
Check Design Rules
View HDL Functional Model
View HDL Instantiation Template
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start
Design
Files
Libraries
Console
1
2
3

```
INFO:HDLCompiler:1574 - Analyzing Verilog file \"C
```

3.12 Program FPGA

We will use the JTAG interface to program the FPGA. While normally separate separate from the FPGA board, the USB-to-JTAG interface is conveniently built into our starter board.

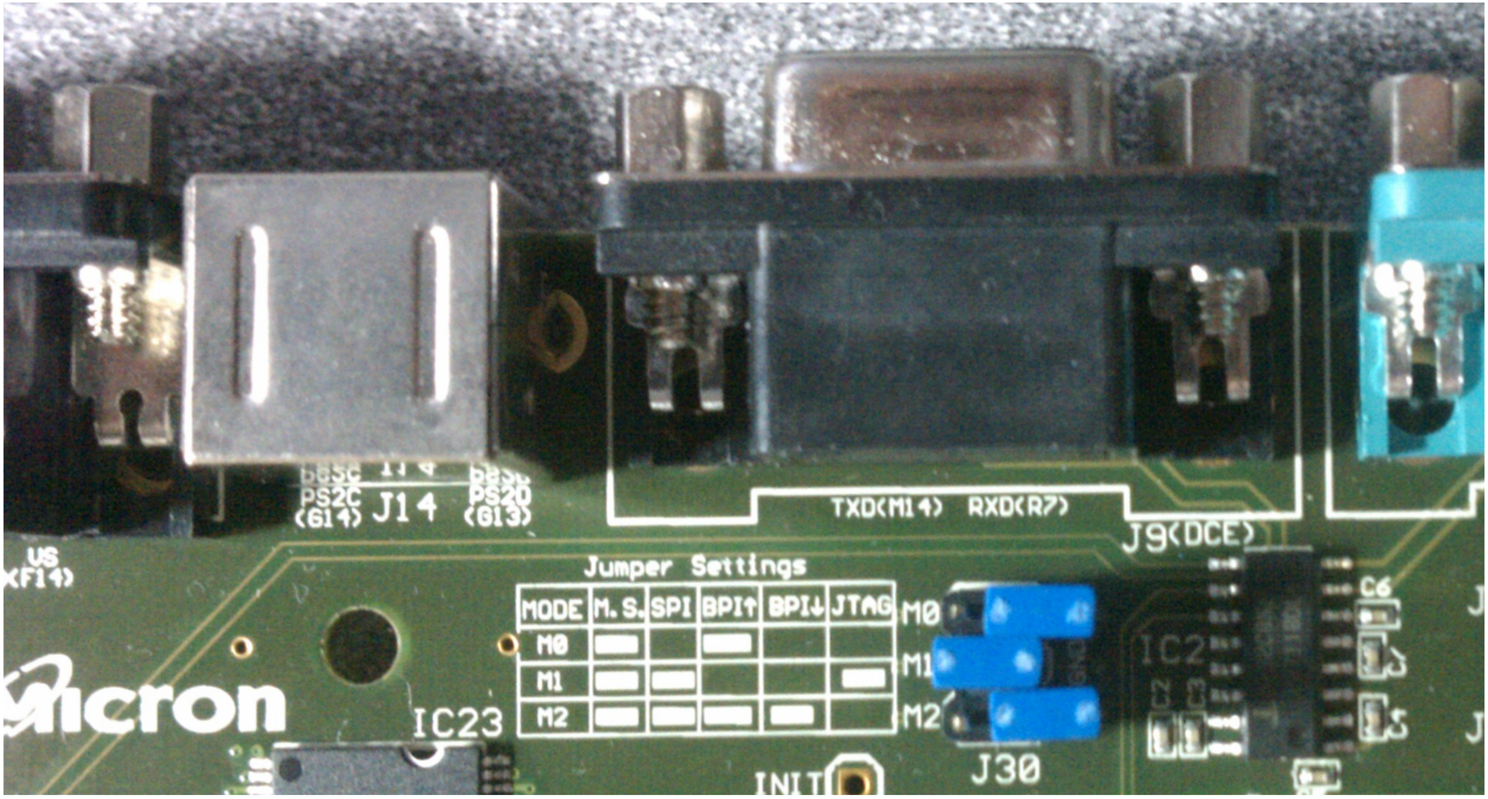
1. Set Jumper J30 to JTAG Setting

    M0=open

    M1=short

    M2=open

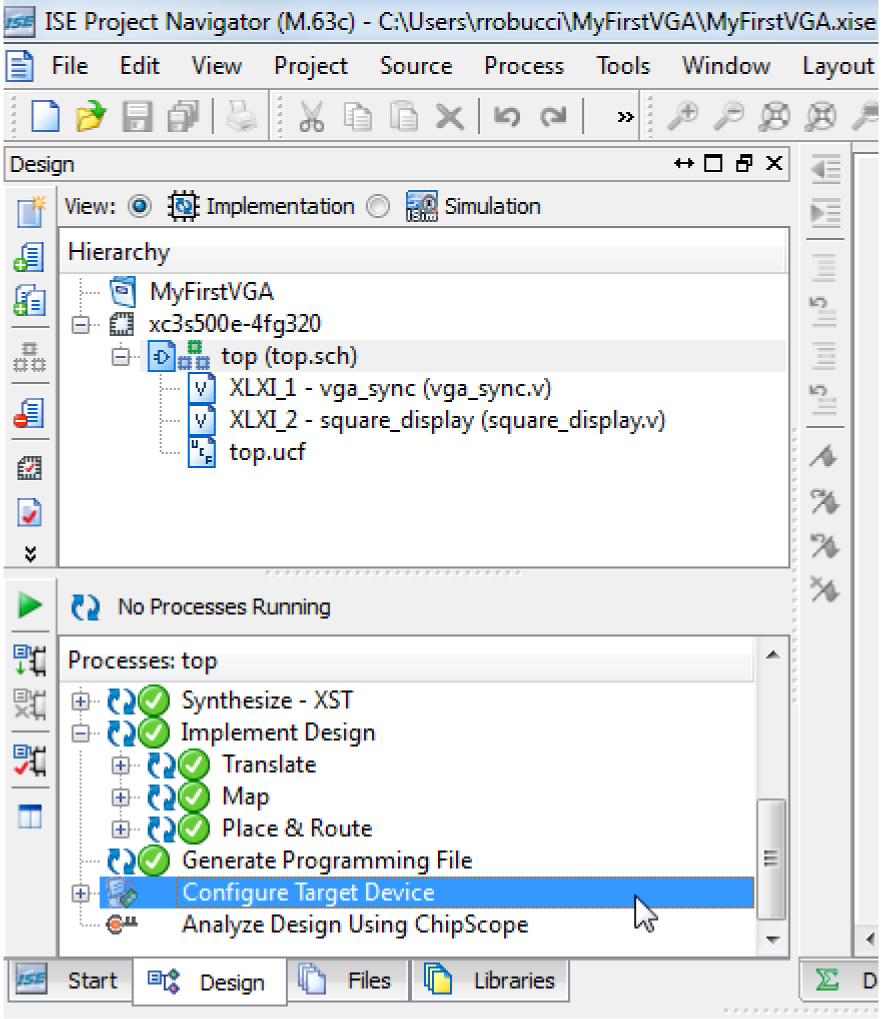
DO NOT DISCARD JUMPERS, JUST PLACE THEM SO THEY ARE ATTACHED TO ONE PIN TO CREATE OPEN:



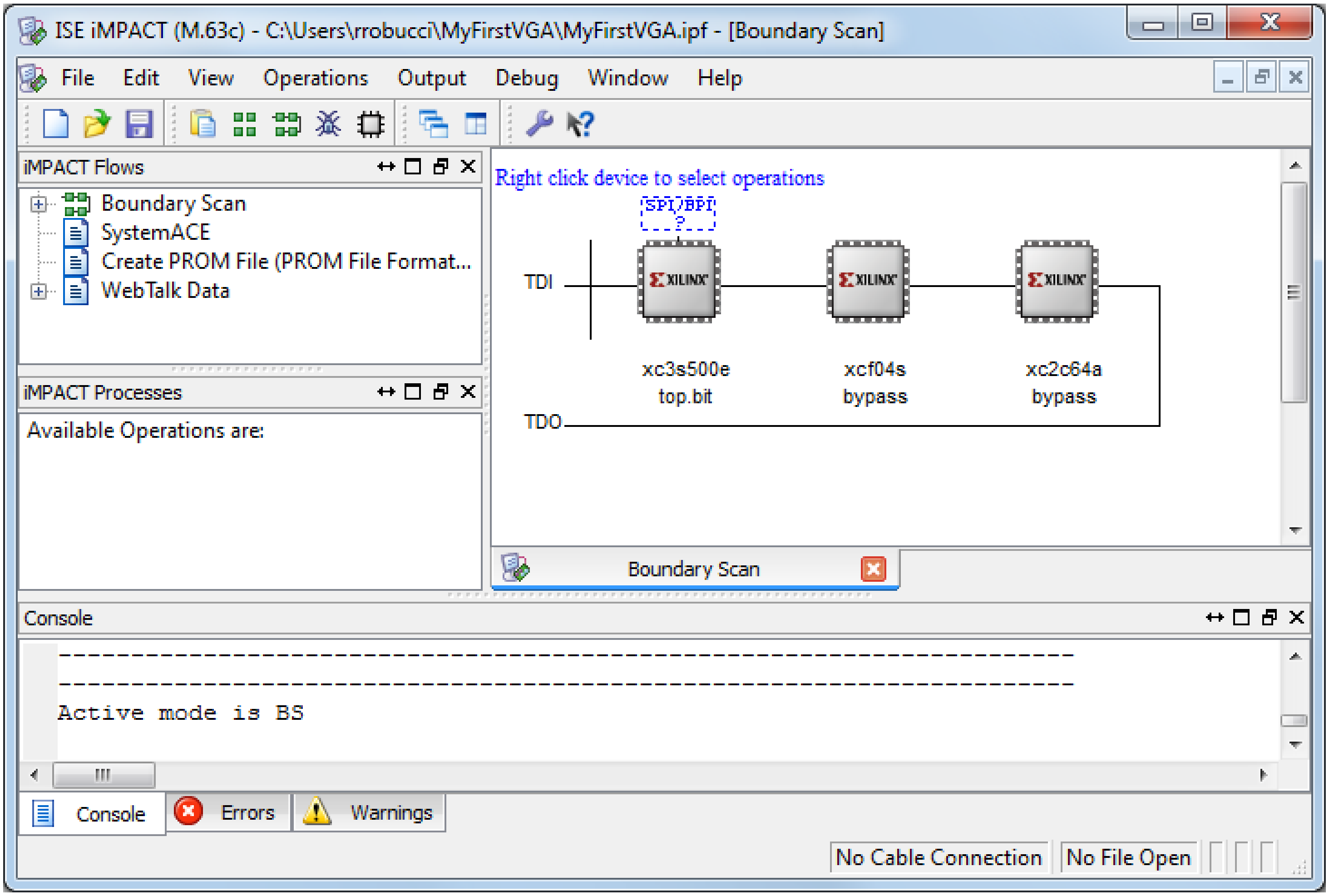
2. Connect USB Cable from board to computer

3. Plug in the board's power adaptor to the board's power connector and a 120 V outlet. Turn on the board using the power switch near the power connector.

4. Double-Click "Configure Target Device" under "Generate Programing File"


ISE Project Navigator (M.63c) - C:\Users\rrobucci\MyFirstVGA\MyFirstVGA.xise
File
Edit
View
Project
Source
Process
Tools
Window
Layout
Design
View:
Implementation
Simulation
Hierarchy
MyFirstVGA
xc3s500e-4fg320
top (top.sch)
XLXI_1 - vga_sync (vga_sync.v)
XLXI_2 - square_display (square_display.v)
top.ucf
No Processes Running
Processes: top
Synthesize - XST
Implement Design
Translate
Map
Place & Route
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
Start
Design
Files
Libraries
D

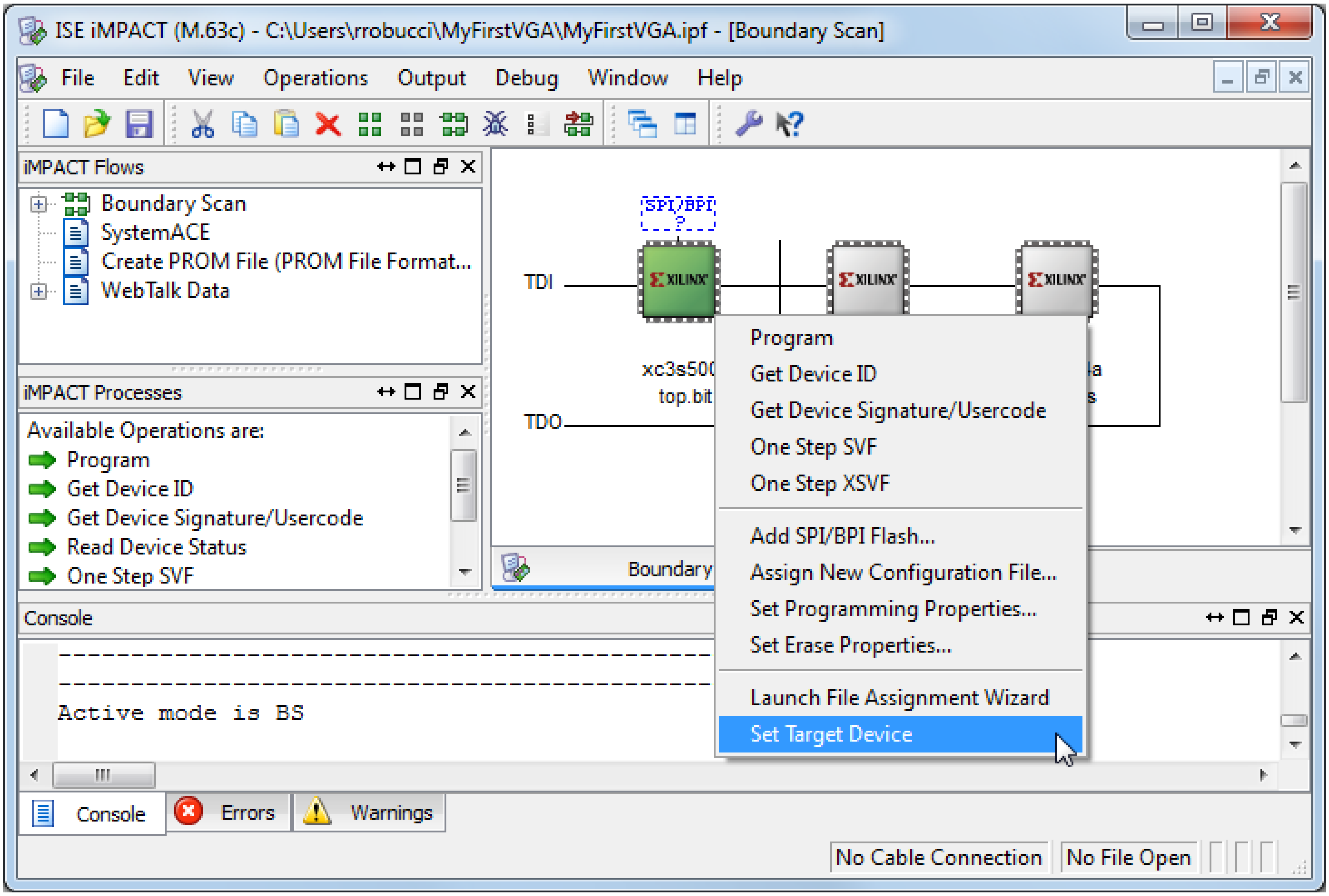
Result:



```
----------------------------------------------------------------------------
----------------------------------------------------------------------------
Active mode is BS
```

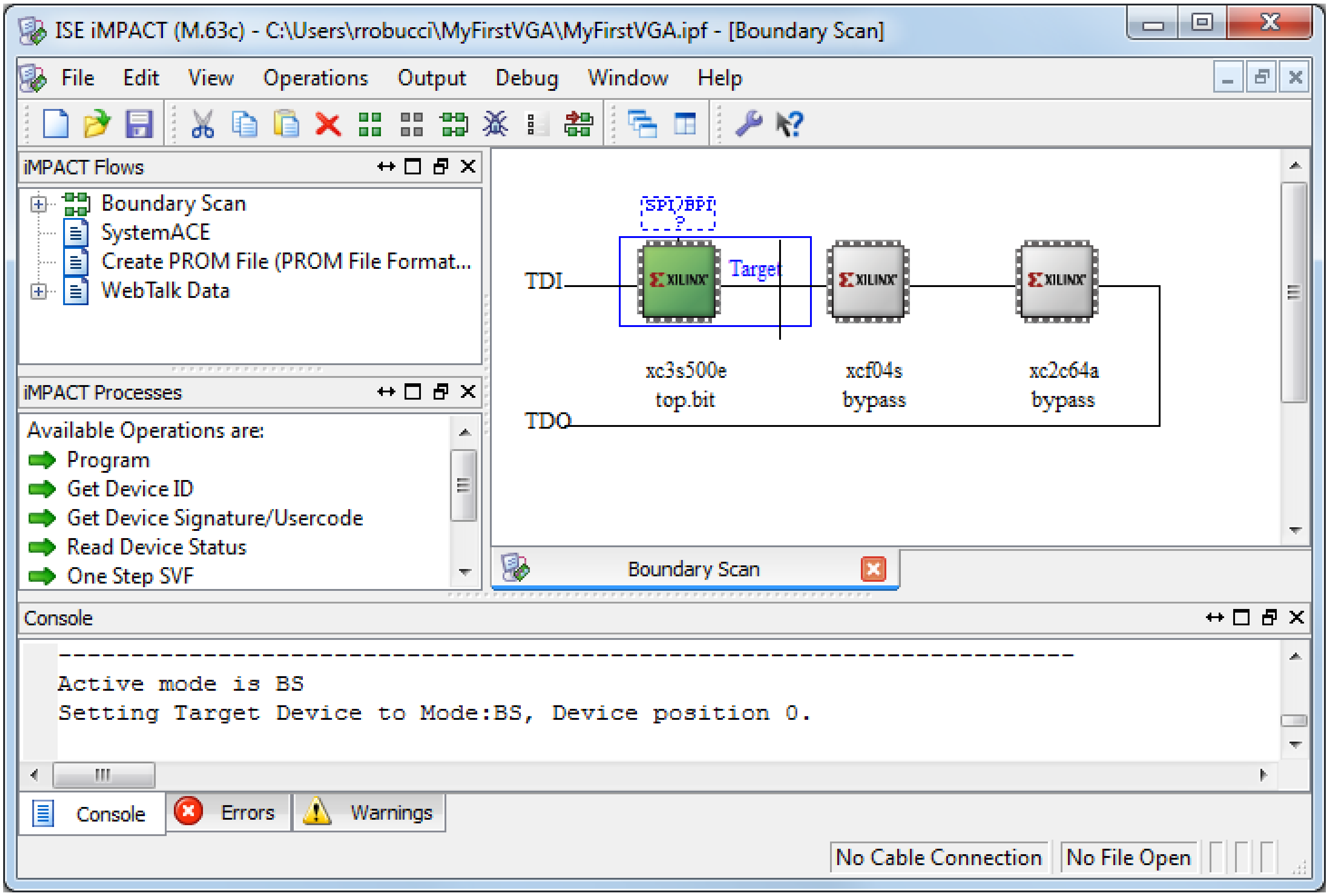
IF YOU DONT HAVE THIS RESULT SHOWING THE DEVICE CHAIN THE FIRST TIME YOU RUN THE TOOL, USE INTRUCTIONS IN SECTION 5 TO MANUALLY START iMPACT, PROGRAM YOUR DEVICE, AND SAVE YOUR CHAIN CONFIGURATION (.ipf file)

5. Right-click the xc3s500e device and select “Set Target Device”



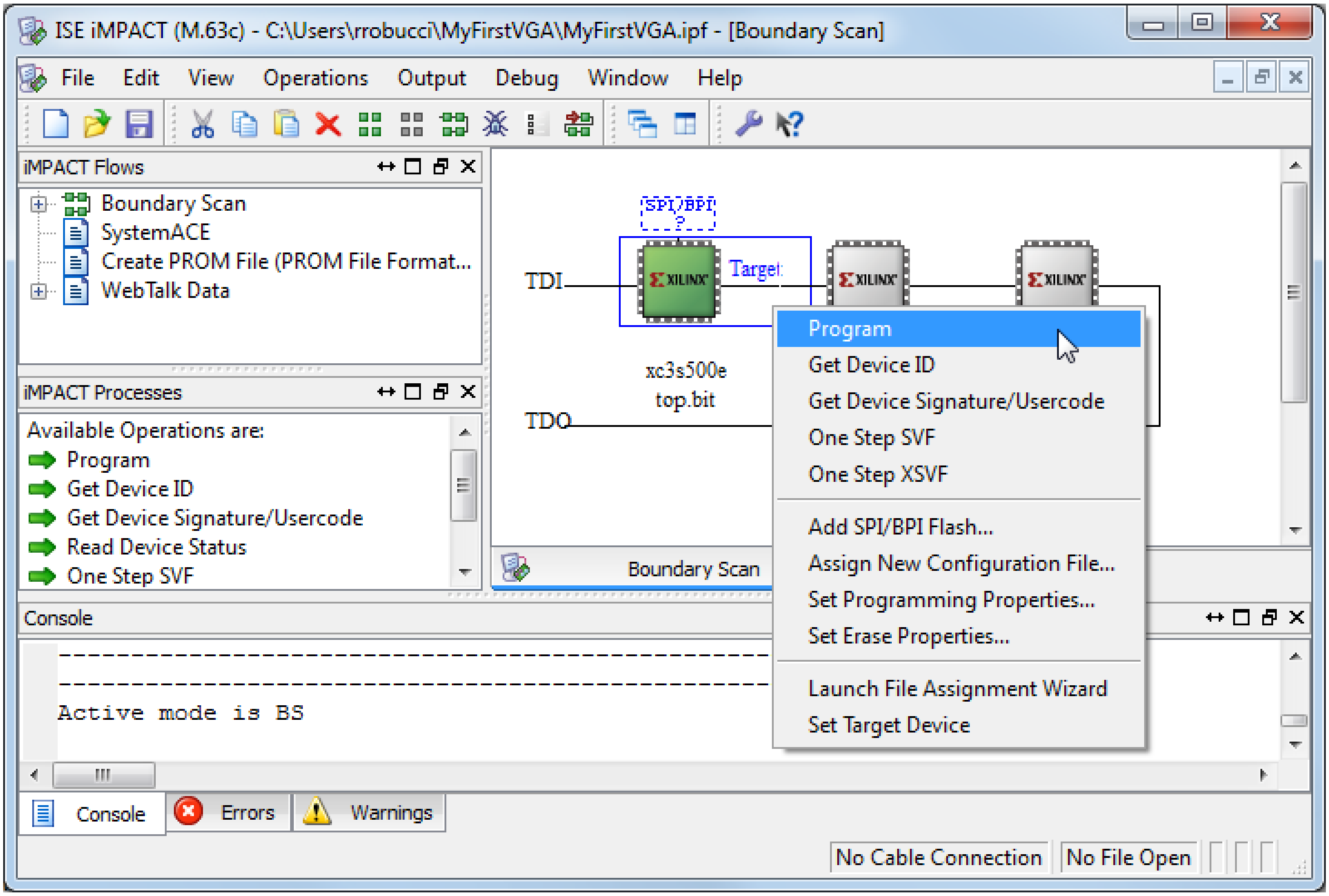
```
----------------------------------------------------
----------------------------------------------------
Active mode is BS
```

Result:



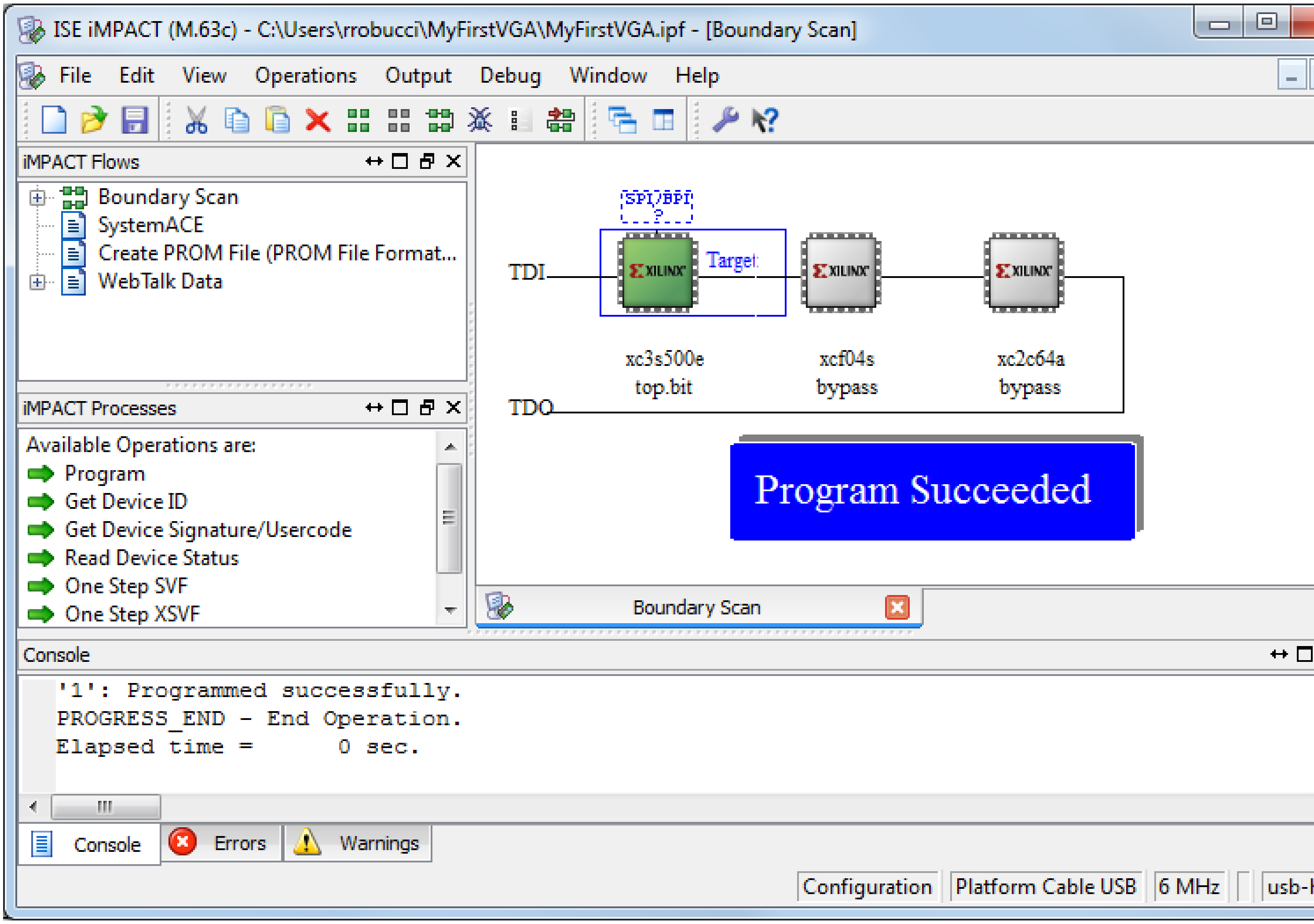
```
----------------------------------------------------------------------
Active mode is BS
Setting Target Device to Mode:BS, Device position 0.
```

6. In iMACT, goto File->Save Project so that you aren't prompted to do this again when starting iMPACT.



```
-----------------------------------------
-----------------------------------------
Active mode is BS
```

Result:



Program Succeeded

```
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      0 sec.
```

3.13 Connect to Monitor

Connect a VGA cable to the starter board and a monitor. You should see a magenta/purple rectange on a blue background.

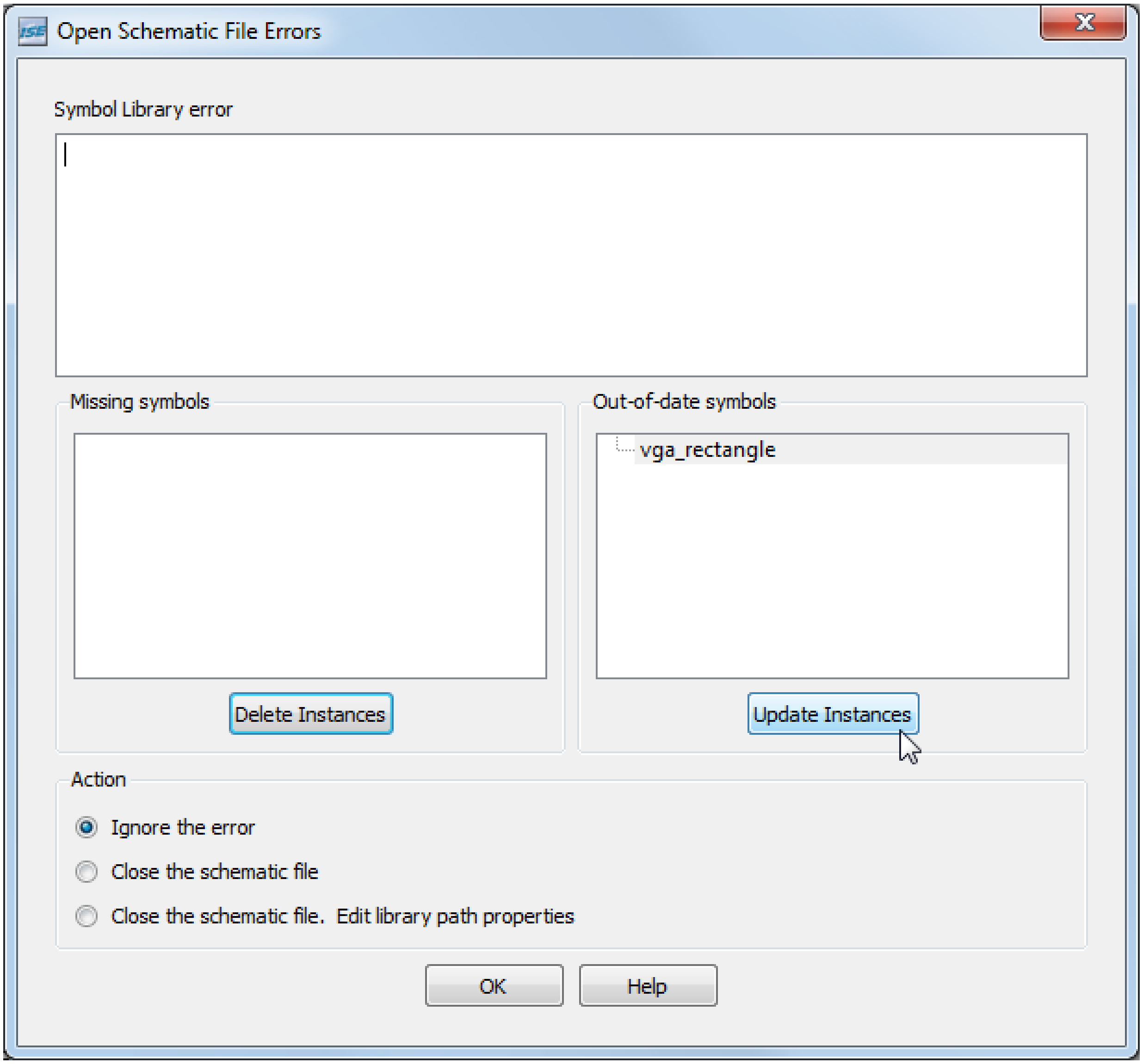
4 Your Design Assignment:

Modify the design to have the ability to change the color of the rectangle and set the background to black based on switch positions.

- The color should be determined by turning on one of threee switches, otherwise the rectangle is black.
- The three switches should correspond to yellow, cyan, and magenta. Having more than one switch on at a time is a "don"t care" condition.

The board's user manual provides a color chart in the VGA port section. It also provides and all the pin location information needed to add the appropriate information to your *user contrainsts file* for the switched.

NOTE: When you update the port definitions of a module, you need to manually regenerate the symbol by running "Create Schematic Symbol" again. When you reopen a schematic with that symbol, it will present you withe the option to update them. Just click "Update Intances".



vga_rectangle

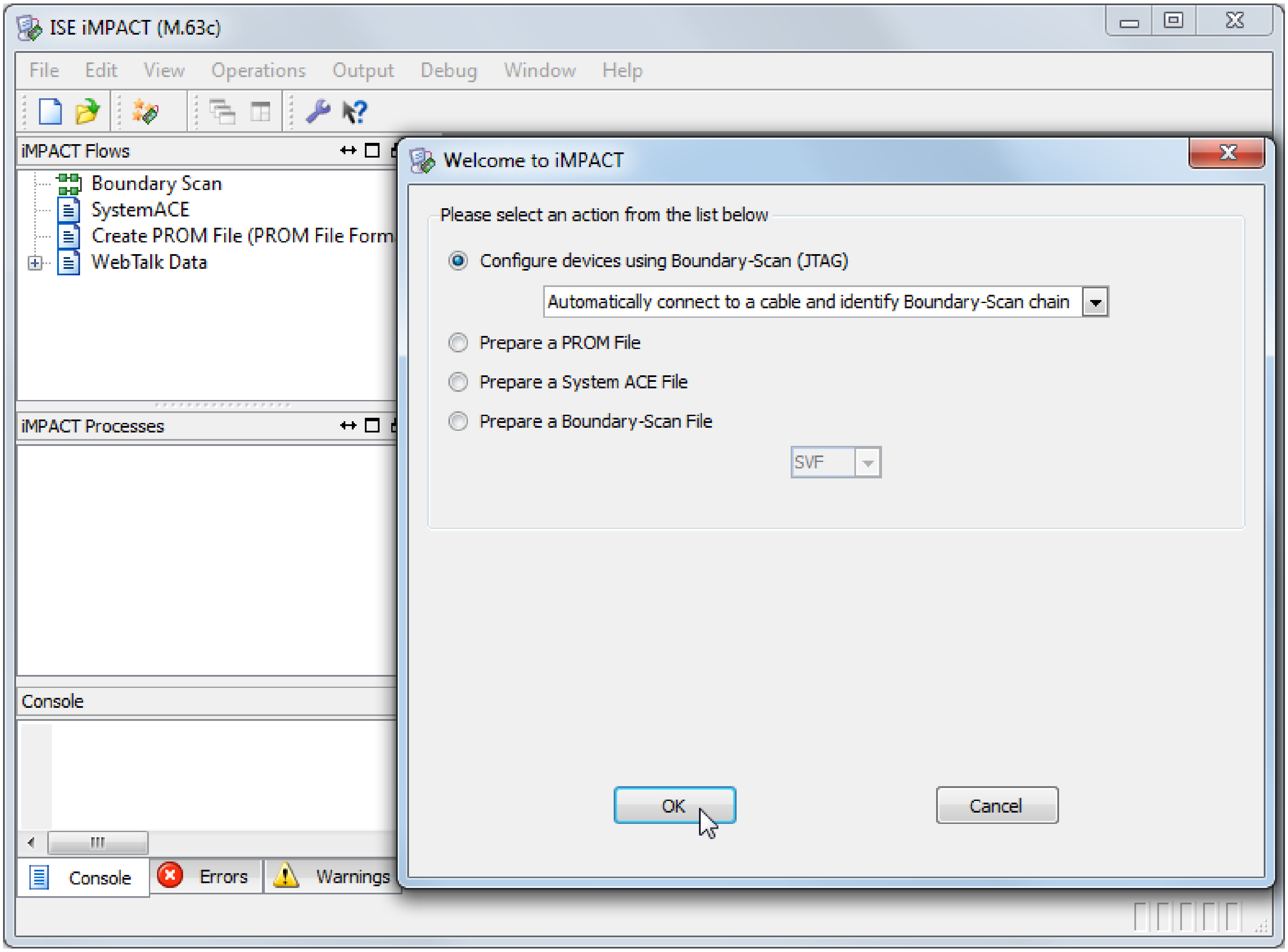
● Ignore the error

○ Close the schematic file

○ Close the schematic file. Edit library path properties

5 Running iMACT Manually

1. In ISE main menu: Tools->iMACT. Reply Yes/OK to any prompts.
2. In iMPACT menu, Edit->Launch Wizard...



Please select an action from the list below

● Configure devices using Boundary-Scan (JTAG)

Automatically connect to a cable and identify Boundary-Scan chain

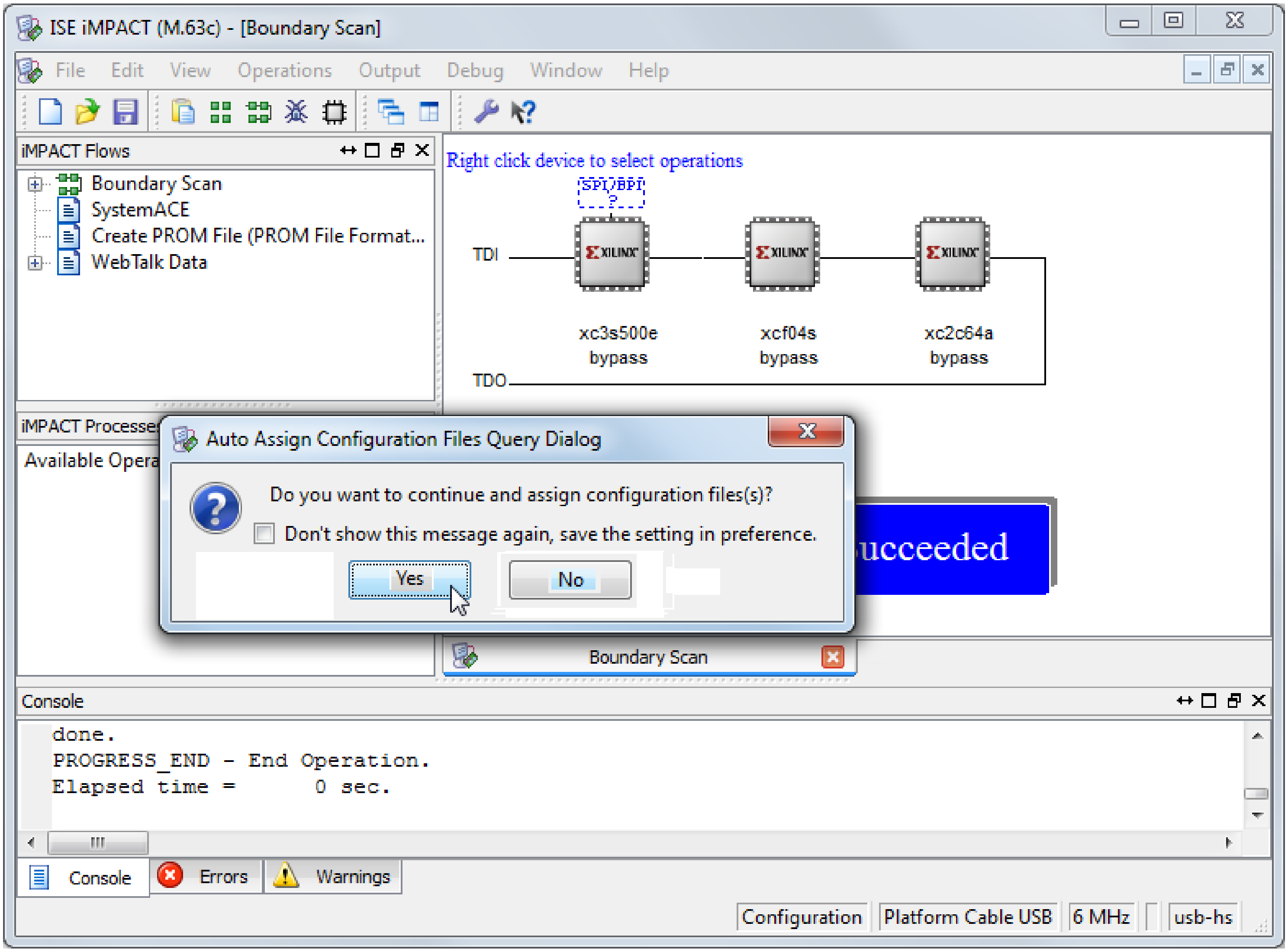
○ Prepare a PROM File

○ Prepare a System ACE File

○ Prepare a Boundary-Scan File

SVF

3. Click OK
4. Click YES in following window.



Auto Assign Configuration Files Query Dialog

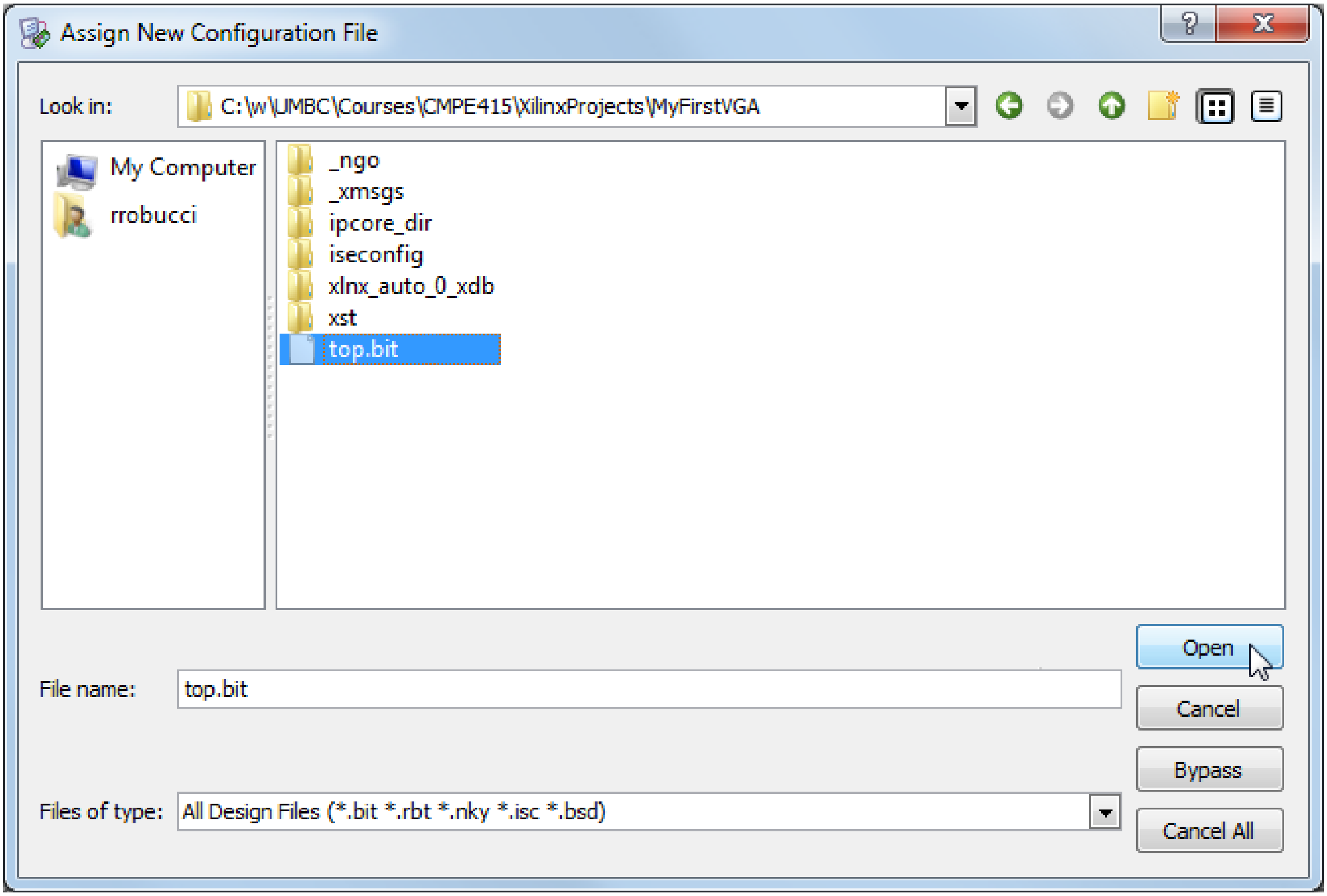
Do you want to continue and assign configuration files(s)?

□ Don't show this message again, save the setting in preference.

```
done.
PROGRESS_END - End Operation.
Elapsed time =       0 sec.
```

Configuration | Platform Cable USB | 6 MHz | usb-hs

5. Select your bit file:



Assign New Configuration File

Look in: C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

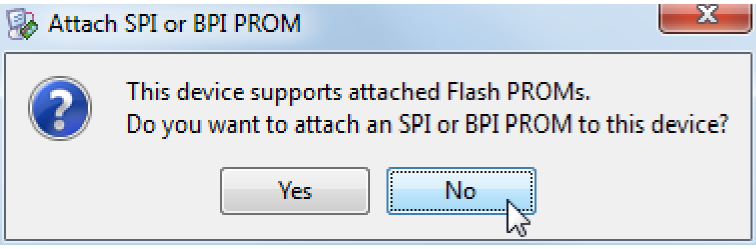
My Computer
rrobucci

_ngo
_xmsgs
ipcore_dir
iseconfig
xlnx_auto_0_xdb
xst
top.bit

File name: top.bit

Files of type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd)

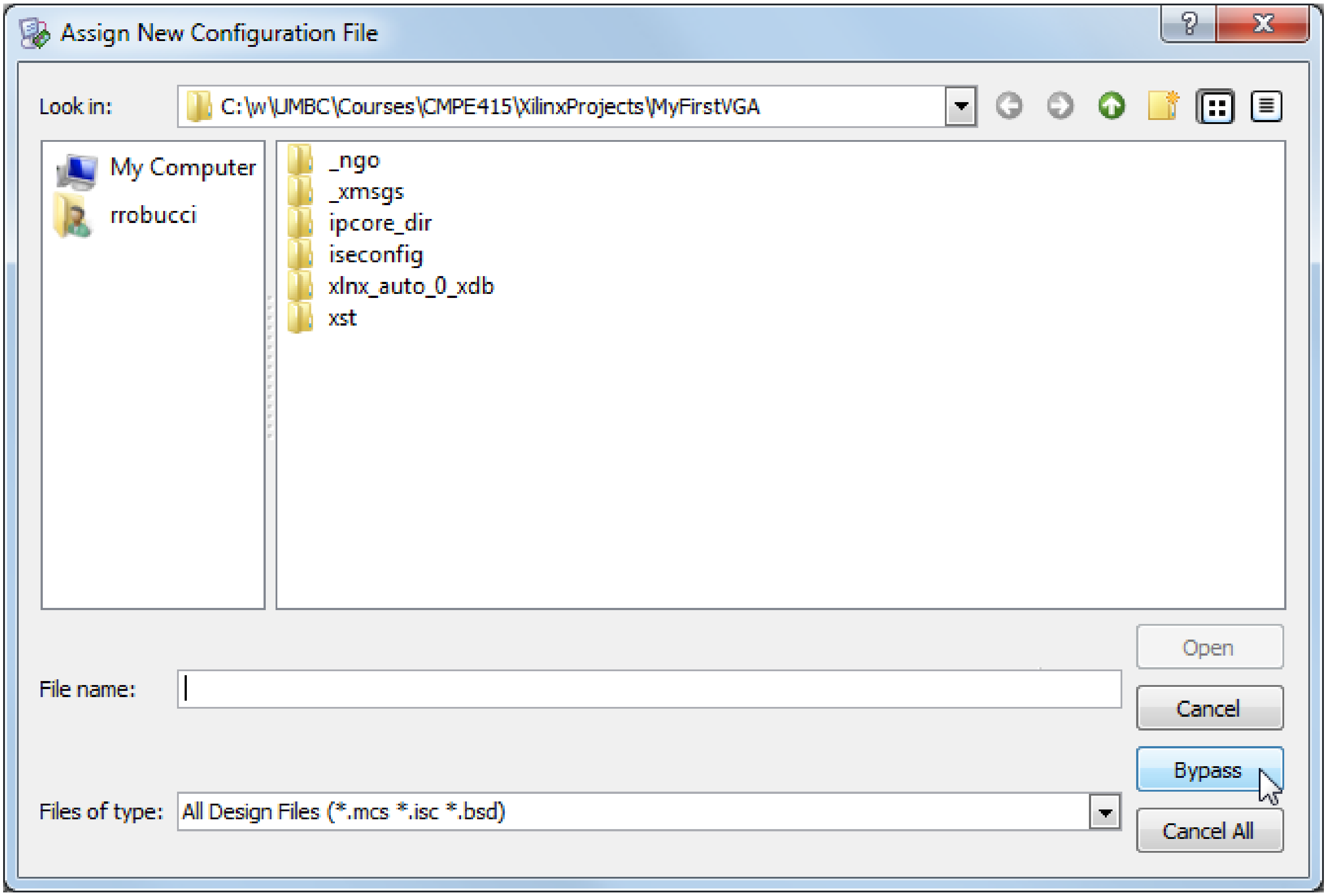
6. Select no (we will not load anything onto the FPGA ROM



Attach SPI or BPI PROM

This device supports attached Flash PROMs.
Do you want to attach an SPI or BPI PROM to this device?

7. For the following two devices, select bypass:



Assign New Configuration File

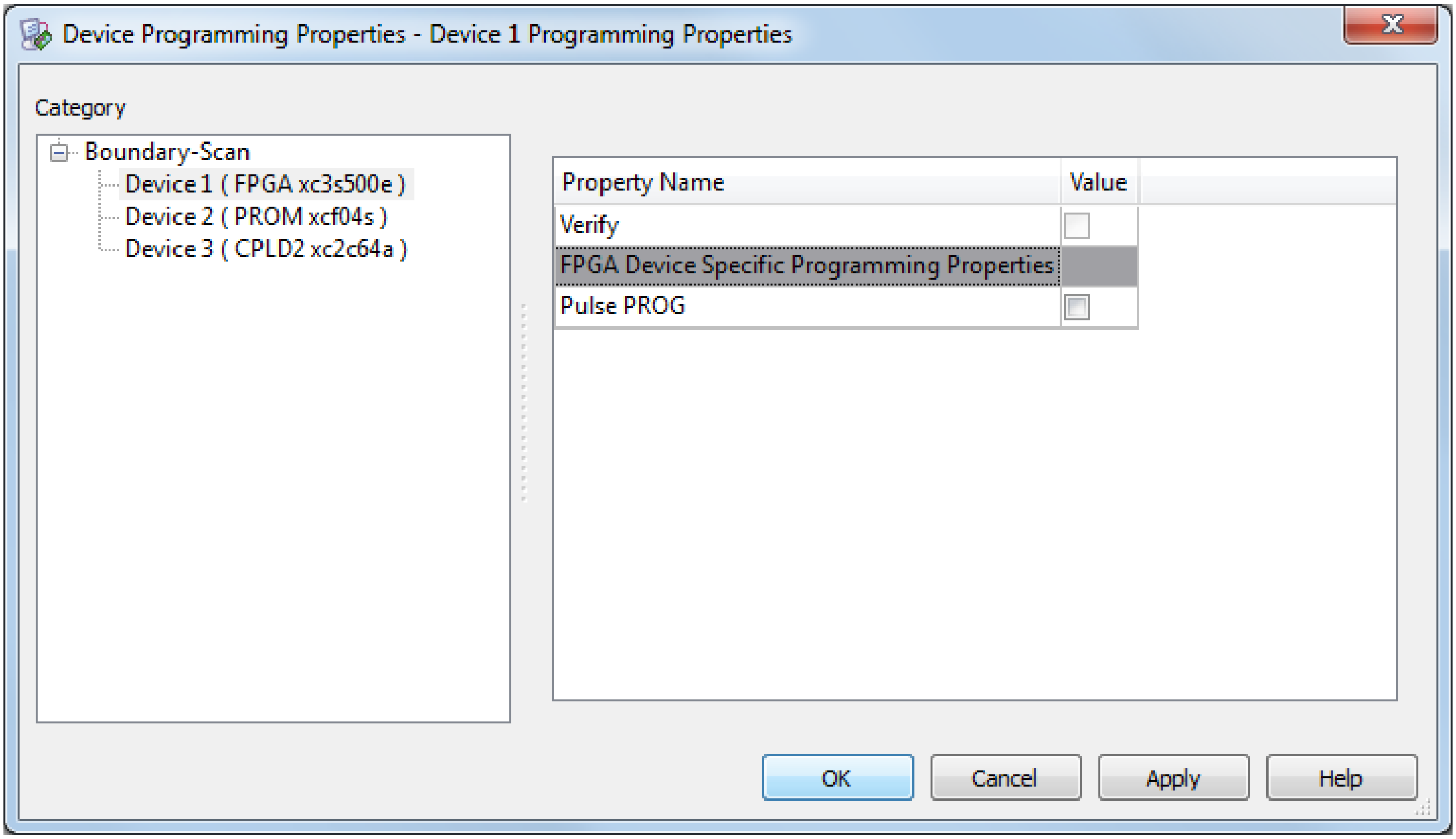
Look in: C:\w\UMBC\Courses\CMPE415\XilinxProjects\MyFirstVGA

_ngo
_xmsgs
ipcore_dir
iseconfig
xlnx_auto_0_xdb
xst

File name:

Files of type: All Design Files (*.mcs *.isc *.bsd)

8. Just HIT OK HERE:



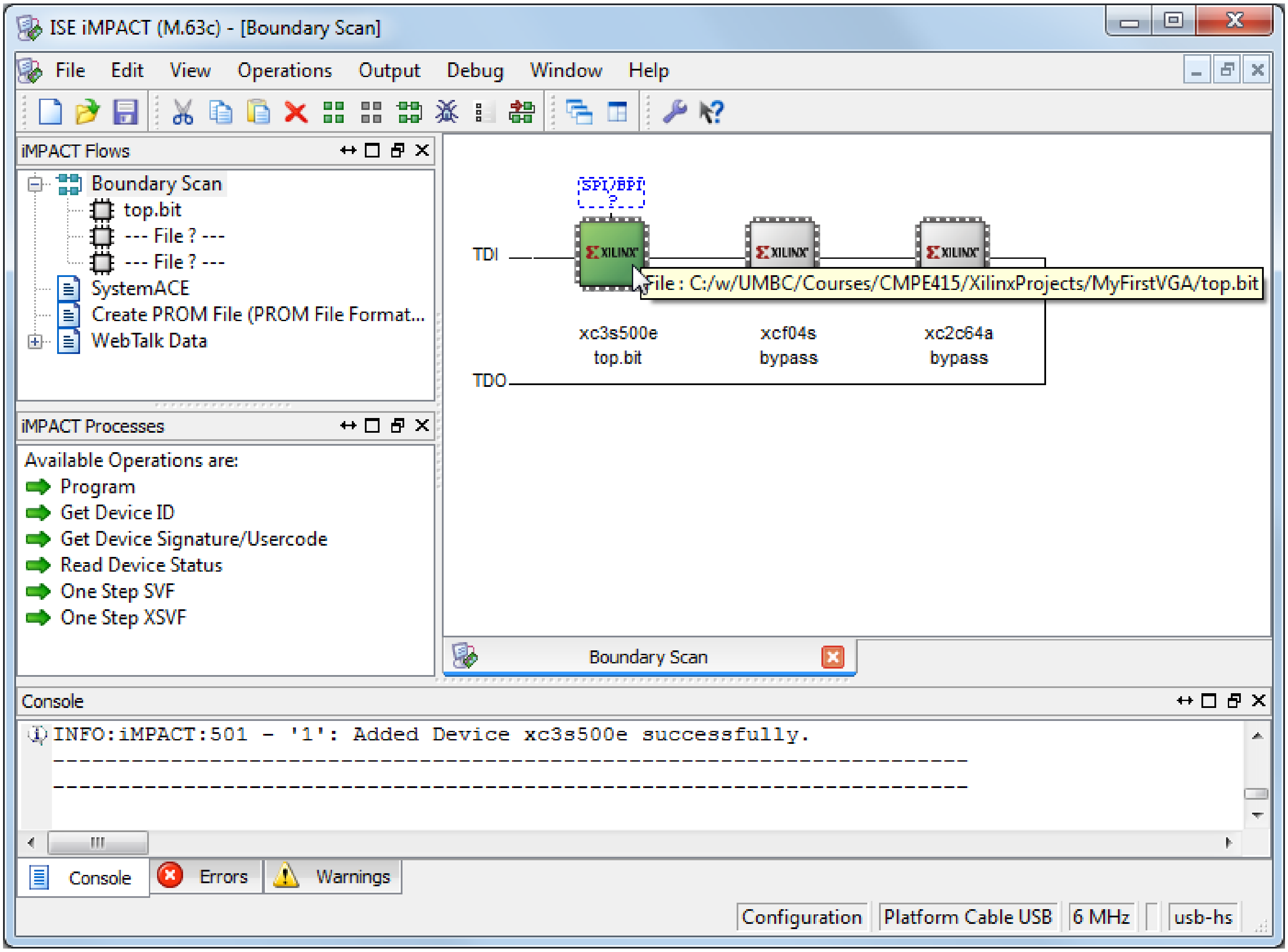
Device Programming Properties - Device 1 Programming Properties

Category

- Boundary-Scan
  - Device 1 (FPGA xc3s500e)
  - Device 2 (PROM xcf04s)
  - Device 3 (CPLD2 xc2c64a)

Property Name	Value
Verify	□
FPGA Device Specific Programming Properties	
Pulse PROG	□

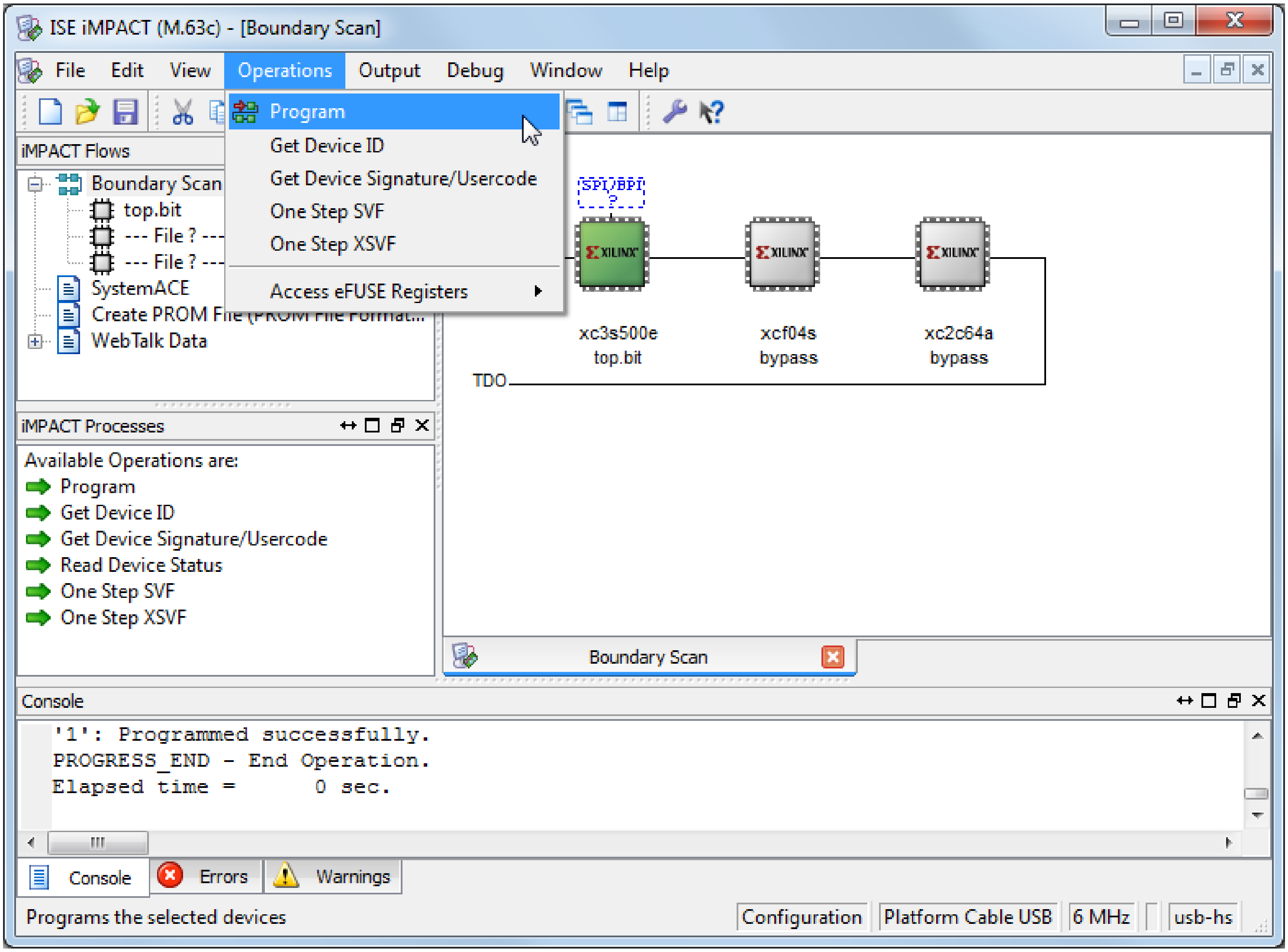
9. Select FPGA device:



File : C:/w/UMBC/Courses/CMPE415/XilinxProjects/MyFirstVGA/top.bit

```
INFO:iMPACT:501 - '1': Added Device xc3s500e successfully.
----------------------------------------------------------------------
----------------------------------------------------------------------
```

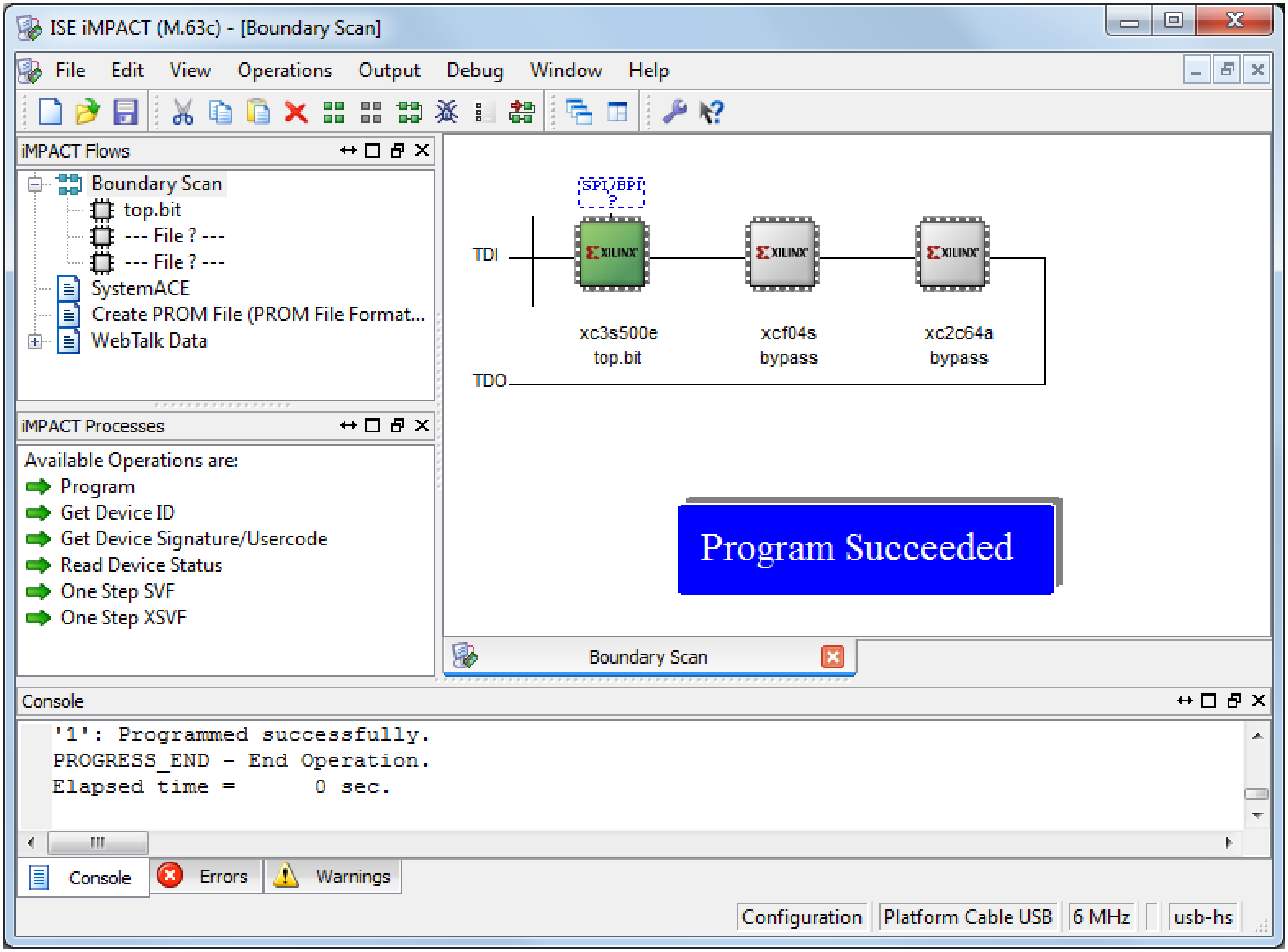
10. Program device:



```
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =       0 sec.
```

Programs the selected devices

Result:



```
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      0 sec.
```

11. Use File ->Save Project to save chain configuration.

When you update your programming file (.bit) you may have to reload it by right-clicking the firt device in the chain, the FPGA, and using "Assign New Configuration File."