Set up and run synthesis script using rtl.tcl

1. Always keep the Verilog files and Synthesized files separated. For example, keep them in verilog and synth folders.
2. Copy the sample rtl.tcl to your synth directory
3. Open the script. I placed a "TODO" above every line you need to/should modify
    a. Path for your Verilog code, change the location between the curly braces { }, to your working directory,
    ex. set attribute hdl_search_path {/data/eehpc0/bisasky/testDir/verilog}
    b. Set myfiles - List all of your Verilog files between the square brackets [ ]. Do not include test files.
    c. Set basename – Add the name of your top level module. Or if you only have one Verilog module, name that module
    d. Set myclk – Leave as clk unless you use a different name for clock
    e. Set myPeriod_ps – Set the clock period. Leave at 1 GHz/1000 ps as a default. Can later increase/decrease that number to adjust the speed/power/area
    f. Additionally, there's "set_attribute lib_search_path {}" and "set_attribute library {}" which have the path and library names. They presently have 3 libraries/paths listed each. The first is library for the standard cells which will be used. The second and third and the libraries for SRAM modules which will not be used. I left them in case you need to use the SRAM modules in the future.
4. Run the script by typing in your synth folder:
    a. rc09 –f rtl.tcl (note: rc09 is an alias name for the rc command, you need to do which rc or which rc09 to understand where is it running from.)
    b. Open the rc.log file and check for any errors (search for "error"). Warnings are generally ok.
    c. If it ran successfully, you should see many files added named after your basename.
    Ex. top.pow, top.sdc, top.cel, top_synthesize.v
5. Troubleshooting errors:
    a. Check the rc.log for errors.
    b. You're running the script in your synth folder and your files are in the verilog folder
    c. Make sure you modified the tcl script file correctly. i.e. the path to your code is correct, path to libraries and library names are correct, all of your Verilog files are listed, the basename is correct.
    d. If there are Verilog syntax errors, it will point them out to the screen and rc.log.
6. Files generated
    a. .area- approximate area breakdown for each module
    b. .cel - list of standard cells used and approximate area and area breakown
    c. .pow – approximate power consumption
    d. .sdc – timing file, used in Encounter layout
    e. _synthesize.v – RTL Verilog file to be used in Encounter layout

    f. .tim – Time to complete the critical path and the timing slack based on the clock period set in the rtl.tcl file. If there is a negative slack, then the clock period is set too low
7. Fine tuning – there is a balance between the clock period set in the rtl.tcl and the power/area. A lower clock period will increase the clock speed but also increase the area and power.