CMPE 641: Topics in VLSI

Course Instructors

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Lecture

TuTh 1-:2:15 pm

Office hours

After lecture or by appointment

Webpage

http://www.csee.umbc.edu/~tinoosh/cmpe641/

Check frequently for class news, handouts, papers, and assignments.

Prerequisites

CMPE 315, CMPE 415 or their equivalent from other schools

Grading: Letter

65% Homework/minor projects
30% Final project and presentation
5% Classroom participation

Course Description

This course introduces VLSI design of application-specific integrated circuits (ASICs) from conceptual design through design release to a foundry using HDL and modern design automation software. Tradeoffs and design perils will be discussed at various phases of this design process. Discussions will include design considerations and tradeoffs made by engineers throughout this process including ASIC performance, power, time to market, design for test, design for manufacturability, etc. Lecture will be accompanied with ample lab time for a hands-on project using the Cadence tool suite including, synthesis of digital circuits using standard cells, static timing analysis, design for test (test generation/fault simulation), floor planning - placement and routing, clock tree insertion and design rule checking.

General Course Description & Objectives

Through this course, students will develop the necessary skills to design systems suitable for numerically intensive processing with an emphasis on ASIC implementation flow. Specifically the objectives for this course are:

- Understand challenges with designing very large-scale chips. Understand challenges with deploying new semiconductor technologies.
- Learn industry standard ASIC design flow.
- Learn how to constrain and optimize the Design in Synthesis and layout.
- Learn how to insert testing techniques for verification of the design

Texbook

For this course, not a specific reference book is required. The best readings come from Cadence manual for different tool that students will explore. Slides will be used in class which covers most of the material. Also for new topics research papers are used as reference.

For basic digital design and RTL verilog this book is suggested

- Digital Design an Embedded Systems Approach Using VERILOG, Peter J. Ashenden, ISBN: 978-0-12-369527-7, Morgan Kaufmann, 2008.

Other helpful textbooks are listed below:

- Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure"

- Golshan, Khosrow, "Physical Design Essentials: An ASIC Design Implementation Perspective" Springer; 2007.
- Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis: Using Synopsys Design Compiler, Physical Compiler, and Prime Time," Springer; 2nd edition (December 1, 2001)

Disabilities

Students who are covered under the American Disabilities Act should inform the teacher privately of this fact at the beginning of the class so that appropriate instructional arrangements can be made.

Academic integrity

Cheating in this course will cause you to fail the course. You are encouraged to consult the instructor if you have any questions on homework, projects and/ or exams. By enrolling in this course, each student assumes the responsibilities of an active participant in UMBC's scholarly community in which everyone's academic work and behavior are held to the highest standards of honesty. Cheating, fabrication, plagiarism, and helping others to commit these acts are all forms of academic dishonesty, and they are wrong. Academic misconduct could result in disciplinary action that may include, but is not limited to, suspension or dismissal. Consult the UMBC Student Handbook to read the full Student Academic Conduct Policy.

Late work policy

If assignment is reviewed in class, no credit is possible for late work. If assignment was not reviewed in class, there will be a 1/3 reduction of remaining credit per day (i.e., 100% -> 67%, 44% -> 30% ...).

Regrading policy

Please bring clear grading errors to my attention. Non-obvious grading issues will not be considered due to fairness to all students, and the inherent subjectiveness of grading.