CMPE 641/491 - Homework #5

Spring 2016

1. [100 pts] The purpose of this problem is to familiarize you with the Cadence Encounter Place and Route tool and designing an ASIC chip using standard cell library that is provided. You will use your ALU processor that you designed in HW1 and HW2 (synthesized) and perform all steps to design your chip and report results as follows. Before starting this assignment, you must review all tutorials that have been given in the website. After your design is fully placed and routed, please follow these instructions to perform analysis and report these results:

- Report maximum frequency that the ALU can run.
- Report the power consumption at the maximum frequency.
- Compare the post place and route power consumption number with the power consumption from synthesis of ALU in HW2. Make sure you keep the frequencies the same.
- What is the chip area and logic utilization of your design?
- Fully verify the design if there is any violation after the design is placed and routed.
- In your report place the screen shot of each step (power plan, post place, and post route and post verification if there is violation (with white x))

  More analysis questions might be added.