CMPE 641/491 HW4

Design of Standard Cells

Design the following standard cells using the tools discussed in class. The first number in a multi-input gate refers to the number of inputs and the number following the X refers to the drive strength (e.g. NAND2X4 is a two input NAND gate with 4X the drive strength as minimum sized). Grading will be based on proper sizing and the compactness of the layout. Compactness of the layout will be accessed by measuring the width of each standard cell. Remember the height of each standard cell will be a constant as discussed in class. Sizes for power and ground rails will also be the same for all standard cells. For any cells that use transmission gates use minimum sized transistors for the transmission gate. All of these cells have to be designed as a single standard cell. Only the clock input is available, so you need to complement in your cell for the inverse.

1. INVX1
2. INVX4
3. INVX8
4. INVX16
5. NAND2X1
6. NAND2X4
7. NAND3X2
8. NOR2X1
9. NOR2X4
10. NOR3X2
11. DFFNX1 (negative edge triggered D flip-flop using transmission gates)
12. DFFNSRX1 (negative edge triggered D flip-flop with asynchronous set and reset inputs using transmission gates, you can choose the polarity for set and reset inputs)
13. LATCHNX1 (negative level sensitive latch using transmission gates)
14. LATCHPX1 (positive level sensitive latch using transmission gates)
15. SDFFNX1 (scan equivalent for DFFNX1, as discussed in class a two-input mux is required on the input using transmission gates, the mux inputs are D and SI (scan in), control is SE (scan enable, enabling SI))
16. SDFFNSRX1 (scan equivalent for DFFNSRX1, mux is the same as mentioned above for SDFFNX1)