# CMPE 641/491 HW3

The goal for this assignment is to design a small circuit that requires control state machine and memory using Verilog and also ARM memory core generator. **For both designs, i.e memory with Verilog model and memory with ARM core model you need to perform simulations and report the design statistics using RC compiler for both designs.**

The circuit computes the product of 128 elements 16-bit vectors: a and b; that is a vector p such that pi=ai*bi. The elements of a and b are stored in separate SSRAMS and the result is to be written into a third SSRAM. Assume that computation is started by a control signal, "go" being one during a clock cycle and output control signal, done is to be set to one during the cycle when the computation is complete. Assume a and b are 16-bit values. In your top verilog, you can assume data was written in ai and bi memories initially and then for testing you need to write to the memories and test reading back for a few samples.

**Design**

i. [10 pt] Draw the detailed block diagram with naming the signals

ii. [15 pt] Use a finite state machine (FSM) to generate the control signals to finish the computation. Draw a state transition diagram for your FSM and also a table to show the values of control signals for each state.

For the SSRAM memories:

iii. [15 pt] first write a verilog model for the SSRAM memories and write the verilog for the complete circuit.

iv. [15 pt] Next, redesign the circuit by suing the ARM Memory Core Generator as shown in the class. Instantiate the memories in your verilog design and make appropriate changes to this design.

**Behavioral Simulations**

v. [20 pt] Test both designs using ncverilog.

**Synthesis**

vi. [25 pt] Perform Synthesis using RC compiler for both designs.

Report maximum design speed, the area, power consumption for both designs in a table that can be compared.