# CMPE 641/491 - Homework #2

**Spring 2016**

1. [25 pts] The purpose of this problem is to familiarize you with the synthesis process and to give you a rough feeling for the size of a few simple circuits in our standard cell library's technology. You use Cadence RC compiler to synthesize each of the blocks below. The script reports timing, area, number of cells, and power consumption at the clk speed rate for your design. Please follow these instructions to perform analysis:

   o  For all designs, register the inputs and outputs, and add timing constraint for the clock (e.g 1GHz). Report slack (set-up and hold time if available). If it couldn't make the timing constraint, slow down the clock until it meets the timing. Report delay for each block. This means that your timing report shouldn't have negative slack.
   o  Make sure your design works and can be compiled correctly, however we won't simulate your blocks using ncverilog/ncsim.
   o  For the report, put each of the verilog designs, rc script and their corresponding output files in a separate folder.
   o  **Report results for all circuits in one table in your submitted report**. Put the area, clk speed (that can meet slack), power numbers in a single table so it can be used as a note sheet for your reference in the future.

   **Blocks**

   a) [10 pts] bitwise OR of two 10-bit numbers (10-bit output)
   b) [10 pts] full adder using verilog "&" "|", "^", "~".
   c) [10 pts] full adder using verilog "+".
   d) [10 pts] 8-bit x 8-bit unsigned multiplier (with sign extension). Use "*" in verilog.
   e) [10 pts] 8-bit x 8-bit unsigned multiplier (without sign extension 8-bit output). Use "*" in verilog.
   f) [20 pts] Your ALU design from HW1. The only change that it needs is to add registers to the inputs and outputs.