

λ -Size ITO and Graphene-Based Electro-Optic Modulators on SOI

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(Invited Paper)

Abstract—One of the key devices that convert electronic signals into high bit-rate photonic data is the electro-optic modulator (EOM). Its on-chip design plays an important role for the integration of electronic and photonic devices for various types of applications including photonic computing and telecommunication. Recently, indium tin oxide (ITO) and graphene have attracted significant attention primarily due to their extraordinary electro-optic properties for the design of ultra-compact EOMs to handle bandwidth and modulation strength trade-off. Here we show design details of a high-performance ITO-EOM in a plasmonic silicon-on-insulator hybrid structure. Results show that ITO is capable of changing its extinction coefficient by a factor of 136 leading to 3λ -short devices with an extinction ratio of about $1\text{dB}/\mu\text{m}$. Further numerical device optimizations demonstrate the feasibility for an extinction ratio and on-chip insertion loss of about $6\text{ dB}/\mu\text{m}$ and 0.25 dB , respectively, for a sub-wavelength compact (0.78λ) EOM design using ITO. Utilizing graphene as an active switching material in a similar ultra-compact plasmonic hybrid EOM design yields enhanced light-matter interaction, in which extinction-ratio is 9 times larger than the insertion-loss for a 0.78λ short device. Both ITO and graphene EOMs are capable of broadband operations ($>500\text{ nm}$) since no resonator is deployed.

Index Terms—Electro-optic modulator, silicon nanophotonics, light-matter interaction, metal-oxide-semiconductor, indium tin oxide, plasmonics, and graphene.

I. INTRODUCTION

THE advancement of modern technology is driven mainly by miniaturization leading to higher performance and lower cost. Photonics has been considered as a technology of promise towards making optical computing and next generation internet data rates a reality. The success and on-going trend of on-chip photonic integration anticipates a photonic road map [1] leading to compact photonic integrated components and circuits. Integrated electro-optic modulation has been identified as one of the major means for chip-based optical communication and signal processing [1]–[5]. A waveguide-integrated EOM can be perceived as a transistor with an optical source, drain, and an electrical gate. For instance a silicon-on-insulator (SOI) waveguide receiving a continuous wave optical beam converts electri-

cal data arriving at the gate into an optical encoded data stream. Even though silicon-based EOMs have been demonstrated experimentally, their requirement of large device footprints (in the order of millimetres) due to weak non-linear electro-optic properties fundamentally limits their device performance, circuit integration density, and cost minimization [3], [4], [7]. The modulation strength can be generally enhanced by increasing the light-matter interaction (LMI), which is classically achieved by deploying high-quality (Q) factor cavities [4]. However, such architectures are somewhat impractical for on-chip designs due to their narrow spectral bandwidth, high energy per bit consumption, and long photon lifetimes. In particular, the modulation bandwidth is limited to a few tens of GHz due to high Q-factors in the range of 10–100 k. Furthermore, their temperature-tuning requirement limits the deployment of such resonance-based photonic modulators due to high power penalties [3], [7].

The footprint and bandwidth constrains can simultaneously be overcome by (i) enhancing the optical mode overlap with the actively index-modulated region and (ii) increasing the LMI of the optical mode with the actively index-modulated material via enhancing the electromagnetic field strength [2], [5], [8]–[10]. In this paper, we show that these desired effects can be achieved by deploying a plasmonic Metal-Oxide Semiconductor (MOS) type optical hybrid- plasmon-polariton (HPP) mode, which concentrates part of the propagating mode's field into a nanometer-thin region overlapping with the actively index-modulated material resulting in a deep sub-diffraction limited mode area [11]–[15]. A fundamental design choice for an EOM is the underlying optical waveguide. With the aim for enhanced LMIs, there is a variety of plasmonic waveguides to choose from. However, plasmonic waveguides have a fundamental trade-off between their mode confinement and propagation length. Among them, the HPP waveguide is found to be relatively superior [11], [15]. This hybrid approach of combining dielectric waveguide mode and surface plasmon mode has been proposed and demonstrated to achieve both sub-wavelength confinement and long propagation distances. HPP waveguides have an improved propagation length with deep sub-wavelength mode confinement significantly below the diffraction limit (i.e. $1/50^{\text{th}}$ of the diffraction limit) [11]–[15]. However, the propagation length of an HPP waveguide is significantly shorter compared to conventional dielectric waveguides [16]. Here, the argument and results suggest that choosing separated waveguide and material systems for passive optical data routing and active data switching, can indeed

Manuscript received October 1, 2013; revised December 5, 2013; accepted December 27, 2013.

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Digital Object Identifier 10.1109/JSTQE.2014.2298451

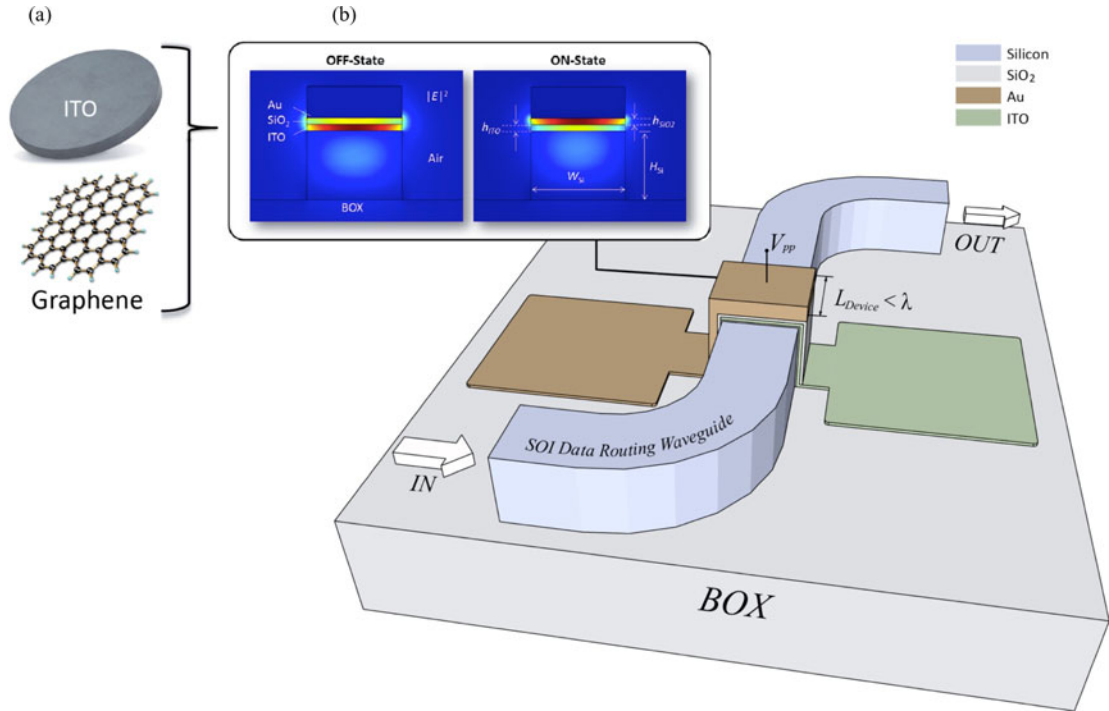


Fig. 1. Schematic of the sub- λ EOM. (a) EO-active materials studied in this paper. (b) The active plasmonic modulation node can be placed arbitrarily into a SOI waveguide platform. The insets show the electric field intensities generated by a numerical finite element solver (Comsol) for the OFF ($V_b = 3$ V, left, $n_{\text{ITO-OFF}} = 1.042 - 0.273i$) and ON-state ($V_b = 0$ V, right, $n_{\text{ITO-ON}} = 1.964 - 0.001i$) of the modulator, respectively. The peak of the electric field intensity is mainly concentrated in the silicon oxide gap in the ON-state and shifts to the strongly absorbing ITO layer in the OFF-state. Notice, the portion of the mode residing inside the silicon core is desired and allows a small impedance mismatch between the MOS switching node and the SOI data routing backbone. The electrical ground can be connected either to the Silicon waveguide or to the ITO, with the latter preferred to avoid additional optical losses of high-doped silicon. A commercial finite element analysis solver (Comsol) is used for the numerical simulations. $\lambda = 1310$ nm.

be accomplished by an SOI and plasmonic hybrid integration architecture [8], [9].

A second important consideration in the design of an EOM is the choice of optically active (i.e., voltage bias-switched) material. Emerging materials with high-modulation capability have been proposed and demonstrated for EO applications [8]–[10], [17], in this paper. For instance, the class of transparent conductive oxides (TCO) such as indium tin oxide (ITO) have been found to allow for unity index changes [8], [9], [18]–[23], which is 3–4 orders of magnitude higher compared to classical EO materials such as Lithium niobate [24], [25]. Since its discovery in 2004, the graphene has become a highly regarded substance in the area of electronics because of its high mechanical strength, electrical and thermal conductivities, and compatibility with silicon [26]–[37]. With its unique optical properties including strong LMI [29], high-speed operation [36] and gate-variable optical conductivity [33], [37], graphene shows a significant potential for electro-optic applications [10], [17].

Here we report on the design and performance of both broadband, ultra-compact plasmonic EOMs based on ITO and graphene (GEOM) integrated into an SOI waveguide platform.

II. DEVICE DESIGN AND PERFORMANCE

The design of our ultra-compact EOM consists of a SOI waveguide with an ITO-SiO₂-Au (or also Al, Cu) stack placed on top, forming an MOS capacitor (see Fig. 1). Key to this design

is the accumulation layer formed in the MOS capacitor at the ITO-SiO₂ interface upon applying a voltage bias between the gold and silicon. ITO's effective index changes from being a dielectric to a quasi-metallic state when a voltage bias is applied. Such design based on the MOS characteristics (i) provides a strong LMI that results in sub-wavelength plasmonic confinement and relatively long propagation distances, (ii) allows the seamless integration into a low-loss SOI data-routing platform, and, (iii) provides a metal contact, which serves as an electrical electrode and heat sink at the same time [8], [9], [11]–[15]. Device dimensions used for the performance optimization include silicon waveguide core width and thickness (H_{Si} , W_{Si}), gate oxide thickness (t_{gate}), ITO thickness (H_{ITO}), and device length (L). For the calculation of the extinction ratio (ER) and insertion loss (IL), following formulas are used

$$ER = \frac{P_{\text{out}}(V_b = V_{\text{OFF}})}{P_{\text{out}}(V_b = V_{\text{ON}})} = \frac{T(L, \Delta\alpha)}{T_0}$$

$$IL = \frac{P_{\text{in}} - P_{\text{out}}(V_b = V_{\text{ON}})}{P_{\text{in}}} = 1 - \frac{T(L, \alpha_{\text{ON}})}{T_0}$$

where P_{out} (P_{in}) is the optical power at the out(in)put of the device, that determines the device performance depending on the geometrical parameters chosen to define the plasmonic MOS mode. Here T is the transmitted optical signal, and

$$\alpha = 4\pi\kappa/\lambda$$

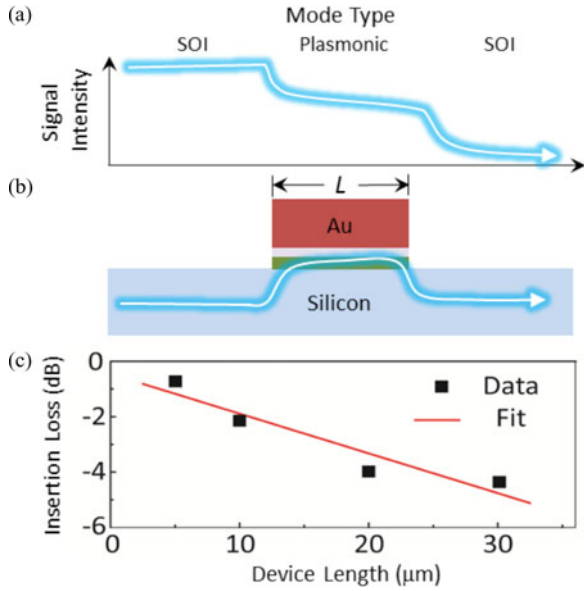


Fig. 2. Insertion loss of the ITO EOM. (a) Qualitative loss discussion. (b) Schematic mode coupling. (c) Experimental cut-back method. The signal intensity drops when light enters and exits the device due to impedance mismatch between the SOI and HPP waveguide section (0.25 dB/coupler). The length dependent loss is 0.14 dB/ μm . Thus, the total loss for a 5 μm long modulator is only about 1 dB. $H_{\text{Si}} = 340$ nm, $W_{\text{Si}} = 800$ nm, $H_{\text{SiO}_2} = 25$ nm, $H_{\text{ITO}} \sim 15$ nm, $H_{\text{Au}} = 350$ nm.

is the incurred loss over the device length, L , where λ is the operation wavelength, κ the imaginary part of the complex effective index of the HPP mode.

By switching the refractive index of ITO via accumulating carriers inside the ITO, the MOS field distribution changes between light-through ON state and the modulator absorption OFF state [see inset Fig. 1(b)].

A particular design challenge is minimizing the insertion loss of the device. Even though the propagation length of plasmonic modes is limited by the ohmic losses, the overall EOM loss can be acceptable if sufficient EO switching can be achieved over just a few micrometers. Therefore, instead of deploying an all-plasmonic circuit, the low loss SOI waveguide infrastructure is used in our design to route the optical data to the λ -scale plasmonic switching element – the EOM (see Fig. 2). Note that the device length, L , in this paper defines the length of the hybrid plasmonic waveguide section only [see Fig. 2(b)].

There are mainly two types of losses, (i) a length dependent loss, which is the insertion loss experienced by the HPP mode while propagating inside, and (ii) a length independent loss that originates from coupling between the SOI waveguide and hybrid plasmonic section. Our measurement indicates a low (0.25 dB) loss for each SOI-HPP coupler due to a low impedance mismatch originating from the fact that some of the optical fields of the HPP mode reside in the silicon core portion of the MOS stack. Combined with an approximately 0.14 dB/ μm length dependent HPP propagation loss, the total insertion loss can be estimated by the cut-back method [see Fig. 2(c)]. Fitting the data gives a total insertion loss of about only 1 dB for a 3λ long device, which is significantly lower, compared to photonic EOM architectures. We like to point to the significance of these

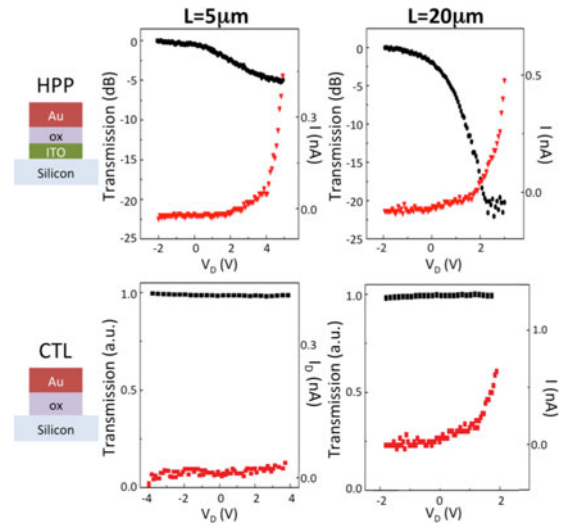


Fig. 3. The experimental modulator performance yields a record-high 1 dB/ μm extinction ratio and is a direct result of the plasmonic MOS mode and the active material's (ITO) ability to alter its optical loss. Increasing the device length, L , results in stronger modulation down to -20 dB for a 20- μm long device. The voltage polarity is chosen such that the gold contact is forward biased (positive pole) while the silicon is grounded. No modulation is observed for reversed bias polarity and when the ITO layer is omitted in the device (control = CTL). The MOS capacitor operation is indirectly verified by a low leakage current of about half a nano-ampere for an applied bias of 3 V (red dots).

results, since they show the feasibility to obtain high efficient coupling to deep diffraction limited optical modes from standard diffraction limited photonics waveguides. An in depth study of this effect on a variety of plasmonic waveguides would benefit the field greatly.

The experimental DC performance of this electro-optic modulator of various lengths shows an extinction ratio of 5 and 20 dB for device lengths of 5 and 20 micrometers, respectively (see Fig. 3 HPP). This high performance, 1 dB/ μm of the device is a direct result of both strong optical confinement of the MOS mode [8], [9] and the capability to change ITO's optical refractive index and loss under electrical bias [18]. Diffraction limited photonic EOMs achieve about 10^{-3} – 10^{-4} dB/ μm [3], [4], [7]. In control samples where the ITO layer is omitted, no beam modulation is observed even for longer devices up to 30 μm in length (CTL in Fig. 3). Notice, that the leakage current levels of the MOS capacitor are relatively low (<0.5 nA), suggesting a good capacitive coupling and successful formation of the MOS accumulation layer.

A. Optical Property of the Active Layer

A key component of an EOM design is the selection of the material and switching mechanism. A promising but mostly unexplored modulation mechanism and material combination is free-carrier and dispersive index-tuning in ITO [20], [21]. ITO belongs to the family of conducting transparent oxides (TCO), which traditionally are deployed in the solar industry as low absorbing electrical contacts [22]. In pioneering work, we have recently shown that the refractive index of ITO can be altered significantly via charge accumulation in MOS-like structures in the near IR frequency range [8], [9].

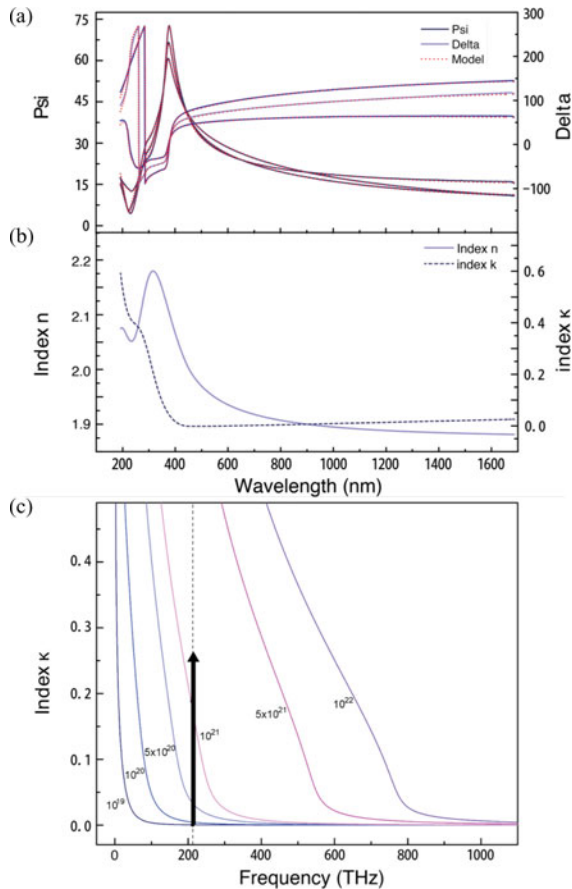


Fig. 4. ITO optical film parameters. (a) and (b) Results from ellipsometry for ON-state ITO films using the general oscillator model as a fit in (a). (c) Imaginary part of the refractive index for the active material ITO based on the Drude-Lorentz model. Arrow indicates voltage-switching range from ON (arrow start) to OFF (arrow tip), respectively [8], [9]. $\lambda = 1310$ nm vertical dashed line

Key for the modulator design is to determine the refractive indices of the ITO film at both the modulator ON (voltage off) and OFF (voltage on) states, respectively. Using ellipsometry, the ON state indices can be determined directly [see Fig. 4(a) and (b)]. Since the top-metal layer shields the ITO film, the parameters in the OFF state are indirectly determined in a 2-step procedure as follows. We first determine the index for as-deposited ITO films via ellipsometry [see Fig. 4(a) and (b)], and then use the optical mode to estimate the index change under voltage bias within a Lorentz-Drude model. Note that the Lorentz-Drude model has been previously utilized to describe the ITO's refractive index [18], [23]. Based on this model, we can map out the real and imaginary parts of the ITO's refractive index $\tilde{n}_{\pi 0} = n - ix$ Fig. 4(c) presents the imaginary part κ for various carrier densities of ITO film. For instance, a highly doped ITO film has a large initial κ value, which would make it challenging to alter κ with high bias voltage. On the other hand, if the carrier concentration of ITO is low, it is easier for us to get a significant κ change. Unlike the main purpose of using ITO in photovoltaic applications, the main aim is here is to obtain a low carrier concentration ITO film during deposition. We successfully demonstrated low- κ ITO films using sputtering, with details to be reported elsewhere [see Fig. 4(b)]. While

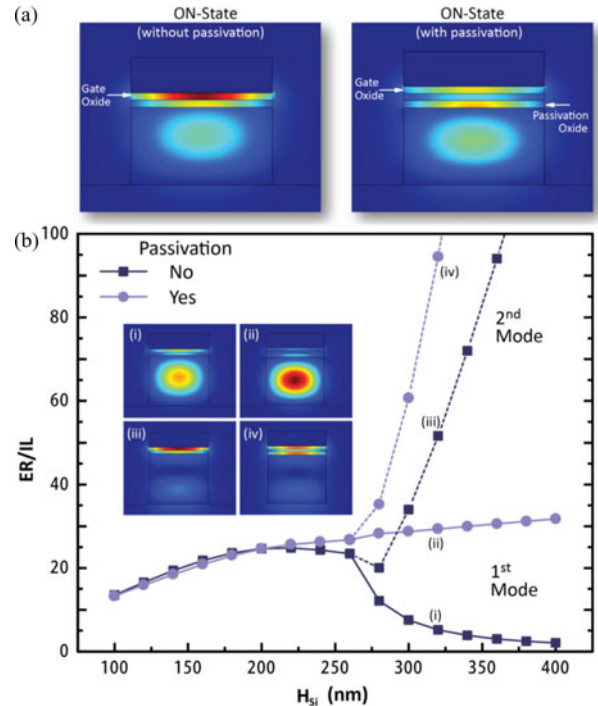


Fig. 5. Effect of passivation layer on the EOM performance. (a) Mode analysis for the ON-state (voltage off) without (left) or with (right) passivation layer. $W_{Si} = 400$ nm $H_{Si} = 220$ nm, $t_{pass} = 20$ nm. (b) Performance compared with/without passivation layer. Solid (dashed) line represents the result with first (second) vertical order mode. ER/IL goes reaches 278 for $H_{Si} = 400$ nm with passivation layer. $H_{ITO} = 10$ nm, $t_{gate} = 20$ nm, $L = 1$ μ m.

the accumulation layer-induced ITO's refractive index profile is non-uniform, the treatment as such is justified three-fold; (a) the ITO index calibration was done for thicknesses of about 10 nm, (b) most of the index change results over a distance of about 10 nm and not more, and (c) this thickness provides for an ideal confinement-loss tradeoff for this plasmonic hybrid mode [13], which is deployed here in this study.

B. Passivation Layer Implementation

Nanophotonic, sub-micrometer sized SOI waveguides are somewhat fragile during clean room processing. To minimize the damage during device fabrication, we introduce a thin, low-dielectric (i.e. oxide) passivation layer [see Fig. 5(a)]. Interestingly, according to an eigenmode analysis (obtained with Comsol solver), the mode effective index of this altered mode is slightly lower than a design without passivation layer. This yields in a relatively lower IL while maintaining ER, due to increased field strength overlapping with the low loss oxide [see Fig. 5(a)]. In the following, we investigate the device performance of an EOM with such added passivation layer.

Rather than focusing on the ER or IL separately, we use the merit of the ER/IL-ratio to track the device performance, where maximization of this ratio is the main goal. In determining the effect of the passivation layer on the device performance, we compared the ER/IL ratio for a 0.78λ long device as a function of silicon core height [see Fig. 5(b)]. The maximum ER/IL ratio is found at the optimal optical confinement, $H_{Si} = 200$ nm,

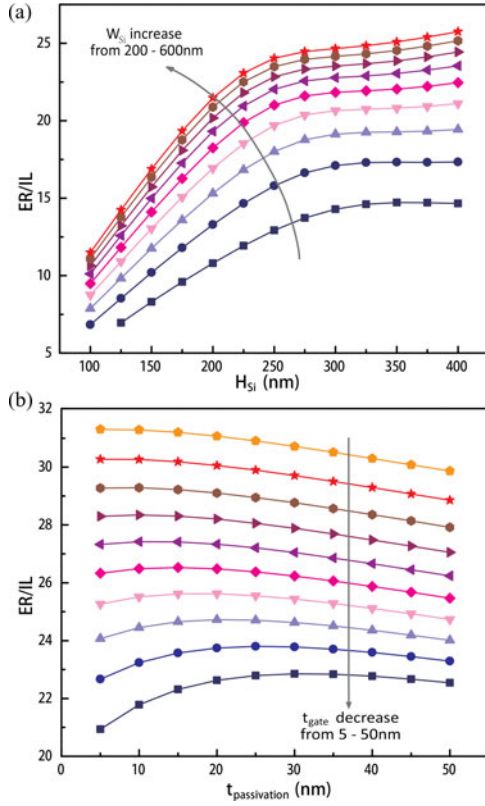


Fig. 6. Passivation-layer effect on modulator performance. In order to achieve better performance, the goal is to increase ER/IL. (a) The performance can be increased by almost 400% by decreasing the Silicon core width and increasing the silicon height. (b) A thin gate- and passivation oxide allows for a strong plasmonic confinement, resulting in high performance values exceeding 30. $H_{ITO} = 10$ nm, $L = 1$ μ m, first-order mode only.

close to the SOI cut-off ($\lambda/2n_{eff} = 218$ nm, $n_{eff} = 3.0$, $\lambda = 1310$ nm). Even though both ER and IL decrease gradually, ER/IL ratio still improves and hence the performance degradation experienced in larger silicon cores is not observed when the passivation layer was added for the 1st order mode. The physical reason for this is that the field has been pushed more into the gap with added passivation layer. Furthermore, at a core thickness of about 250 nm, the second SOI vertical mode emerges, whose top lobe has a significant field overlap with the active material in the gap, thus improving the ER/IL ratio significantly. There are two main mechanisms behind this improvement: (i) upper lobe of the field increases the overlap with the plasmonic gap and hence with the active material, and (ii) the lower lobe gains intensity with more field residing in the silicon core; the former improves the ER, while the latter decreases the IL. This argument also explains the similar trend when a passivation layer is added, as it does not influence the field distribution of the overall mode. Note, that while the performance for the 2nd mode is superior, the actual mode might not be excitable since its real index is significantly (by about 1) lower compared to the SOI index outside the device. This would result in (a) insufficient excitation of the plasmonic MOS HPP mode, and (b) a strong back reflection of at the device input.

Using the hybrid plasmon (HP) design with added passivation layer, we can analyze the performance with respect to the

TABLE I
PERFORMANCE WITH VARIOUS OXIDE MATERIALS

Oxide ^a	Passivation Layer	Insertion Loss	Extinction Ratio	ER/IL
$SiO_2 \sim 1.45$	N/A	0.24	2.19	9.07
$SiO_2 \sim 1.45$	20nm	0.20	1.83	9.19
$Al_2O_3 \sim 1.73$	20nm	0.25	2.64	10.63
$TiO_2 \sim 2.5$	20nm	0.31	4.08	12.96

The unit for both insertion loss and extinction ratio is dB/ μ m. Device length is assumed as 1 μ m. The SOI waveguide silicon core is 400 nm wide and 340 nm high. ^aOxide refractive indices are taken at the wavelength of 1310 nm. Refractive index of TiO_2 is taken as 2.5.

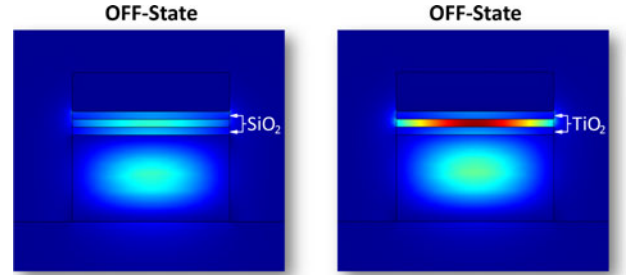


Fig. 7. Comparison of OFF-State modes for EOMs with SiO_2 (left) and TiO_2 . The results have been normalized to the same color legend.

various geometrical device changes (see Fig. 6). Starting with altering the Silicon waveguide core, the modulation performance improves with widening the waveguide (W_{Si}), which can be understood based on the fact that the area of the plasmonic gap has been increased. Thus, more field resides either in the oxide layer at the ON-state or active layer in the OFF-state. Similarly, for the increasing the Silicon height (H_{Si}), the ER/IL ratio increases more gradually, since the confinement loosens.

Two other geometry parameters need to be optimized are the gate oxide thickness (t_{gate}), which controls the electrostatics of ITO accumulation layer in the MOS stack, and the passivation layer thickness ($t_{passivation}$). Decreasing the t_{gate} (here SiO_2) leads to a stronger electric field inside the device resulting in a higher carrier density and hence an increased Δn_{ITO} . Furthermore, decreasing t_{gate} leads to lower IL and ER, and similarly a thinner $t_{passivation}$ results in a higher modulation switching and larger IL. In addition to these geometrical parameters, the permittivity of the oxide material has an effect on the modulation performance as well. Replacing SiO_2 with higher permittivity oxides such as Al_2O_3 or TiO_2 leads to higher ER/IL ratios (see Table I). Increasing the index difference between the ITO and the oxide increases the polarization charges resulting in a stronger optical confinement, i.e. larger overlap factor of the optical HPP mode with the active material in the OFF-state (see Fig. 7). With voltage applied, $\tilde{n}_{ITO-OFF} = 1.042 - 0.273i$, replacing SiO_2 ($n_{SiO_2} = 1.45$) with TiO_2 ($n_{TiO_2} = 2.5$), results in a better field confinement (see Fig. 7).

C. Metal-CMOS Compatibility

Our electrical gate contact made of gold (Au), which is the commonly used material in plasmonics due to its relatively low

TABLE II
PERFORMANCE WITH VARIOUS TOP METALS

Metal ^a	HPP mode Effective Index		Insertion Loss	Extinction Ratio
	On-State	Off-State		
Au 0.31-9i	n = 2.511397 $\kappa = 0.010969$	n = 2.241107 $\kappa = 0.147778$	0.45	5.7
Al 1.232-13.255i	n = 2.430374 $\kappa = 0.012695$	n = 2.188594 $\kappa = 0.134015$	0.52	5.05
Cu 0.512-7.014i	n = 2.612294 $\kappa = 0.041619$	n = 2.309824 $\kappa = 0.18479$	1.73	5.96
Al(n-Cu) 0.512-13.255i	n = 2.431749 $\kappa = 0.005574$	n = 2.190756 $\kappa = 0.129412$	0.23	5.16
Cu(n-Al) 1.232-7.014i	n = 2.587951 $\kappa = 0.092425$	n = 2.283949 $\kappa = 0.216682$	3.85	5.18

The unit for both insertion loss and extinction ratio is dB/ μm . Device length is assumed as 1 μm . ^aMetal indices from ref. [38], $\lambda = 1310$ nm.

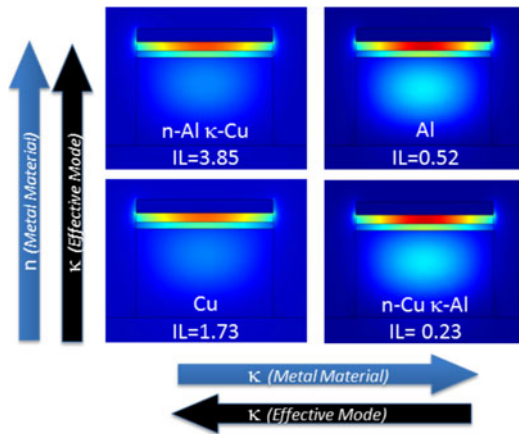


Fig. 8. Modal loss and device performance analysis for various top-metal combinations toward CMOS compatibility.

optical loss [8], [9]. However, gold is not a CMOS compatible material since it introduces deep mid-bandgap traps into silicon. More CMOS compatible metals are aluminum (Al) and copper (Cu).

Here, we investigate the effects of the metal type on the device performance, in particular on the insertion loss. Interestingly, Al leads to lower IL compared to Cu. This is surprising at first, because Cu has lower imaginary index compared to Al, hence suggesting a lower modal loss. This phenomenon, however, can be explained as follows; the loss of the MOS HPP mode deployed here depends not only on the material losses (κ) utilized like in a classical diffraction limited waveguide, but also on the real index (n). Since, the HPP mode originates from polarization charges at the metal-oxide interface, the optical fields are confined inside the low-permittivity (i.e. oxide) gap [11]–[15]. Hence, the field overlapped with the various material components determines the optical loss of the HPP mode.

Next, we compare ER and ILs of devices with Au, Cu, and Al films in the modulator ON-state (see Table II, Fig. 8.). Starting from Cu (lower left), the IL is relatively large. Notice, that a significant amount of optical field resides inside the metal. Increasing the optical refractive index, n , of the metal and keeping κ constant worsens the effect (upper left). This is due to the

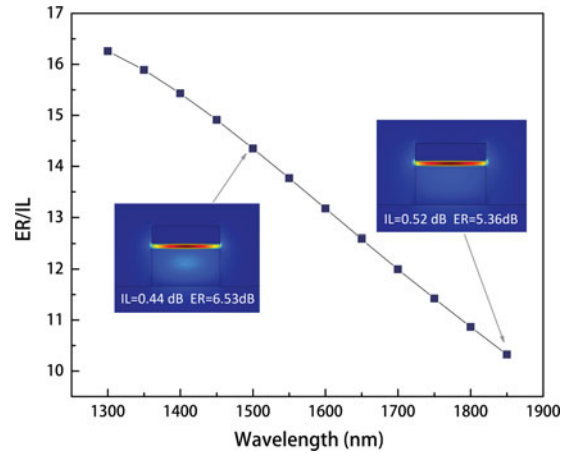


Fig. 9. ER/IL ratio over a wide range of wavelengths for the ITO-EOM. $H_{\text{Si}} = 220$ nm, $W_{\text{Si}} = 400$ nm. First order mode with $t_{\text{passivation}} = t_{\text{gate}} = 5$ nm, $L = 1$ μm . Spectral dependence range [0.3–8.82i to 0.49–12.85i] for Gold after Ref. [38].

fact that the mode confining polarization charges is less pronounced [11], [12]. However, going back to the Cu-case (lower left), but keeping the relatively low refractive index of Cu and artificially increasing to the loss of Al reduces the modal loss significantly (lower right). This can be explained by the same argument as before. Notice that the field inside the metal appears dark blue, indicating minimal field, and hence a low loss mode. The slight performance decrease in ER (from Au to Al) opposes an almost 4 times increase in the loss (from Au to Cu) (see Table II). This analysis concludes that Al is a better choice than Cu for CMOS applications.

D. Wide Broadband Potential

In telecommunication, data and signal routing the scheme of wavelength-division-multiplexing (WDM) has been established as a superior means of delivering high data bandwidths over time-division-multiplexing [12]. Thus, future on-chip platforms and EOMs should be compatible with such methods. Within an ever-expanding wavelength range modulators have to span tens to hundreds of nanometers in bandwidth, in order to avoid challenging and failure prone tuning of individual resonator-based architectures. To this end, we tested this ultra-compact EOM for its broadband operation performance by scanning the wavelength from 1.30 to 1.85 micrometer and track its performance (see Fig. 9). As the wavelength increases, the cut-off Si core thickness increases, thus pushing more field into the gap. Fixing the silicon core height at 220 nm, the field resides more in the plasmonic gap, which causes an increase of IL from 0.39 to 0.52 dB while ER decreases about 1 dB, as shown in Fig. 9. Nonetheless, the ER/IL ratio is still remarkably high over 550 nm bandwidth, demonstrating broadband operation capability. This is possible since no resonator is utilized which supports previous results of the HPP mode [12]. Thus, the device offers to comply with future WDM architectures.

III. GRAPHENE ELECTRO-OPTIC MODULATOR

In the following section we explore a graphene-based EOM based on the plasmonic HPP MOS mode [see Fig. 1(a)].

Graphene, a monolayer material with gate-variable optical conductivity that can achieve strong coupling with light and high-speed operation, is considered as a desired material for future EOM design [33], [37]. Extremely high current density and intrinsic mobility (100 times more than in silicon) make graphene an attractive material to be used in opto-electronics devices [10], [17], [26], [36].

One of the several properties of the graphene under careful examination both theoretically and experimentally is its optical conductivity ($\sigma_c = \sigma_r + i\sigma_i$) in different parts of the electromagnetic spectrum [27]–[33]. A variety of factors determine σ_c : wavelength λ , temperature T , hopping parameter t , and chemical potential μ_c , which is a function of the carrier density and can be controlled by gate voltage, electric field, magnetic field, and/or chemical doping. Li *et al.* experimentally demonstrated the gate voltage dependency of σ_c by measuring the conductivity of a single graphene sheet for the infrared part of the spectrum [33] under different biasing conditions.

Theoretical models for calculating the optical conductivity of graphene differ from each other since different models were utilized and assumptions made. In [27], Gusynin *et al.* developed a frequency dependent electrical conductivity tensor using the Kubo formulation. Peres *et al.* [28] studied the electronic properties of graphene in the presence of defects, and electron-electron interaction as a function of temperature, external frequency, gate voltage, and magnetic field. Wunsch *et al.* [29] and Hwang and Das Sarma [30] developed similar methods to calculate the conductivity of graphene from the polarization based on the Dirac cone approximation for a finite chemical potential and arbitrary radian frequency, respectively. Stauber *et al.* also developed a method based on the Kubo formulation to calculate the optical conductivity of graphene by taking into account its full density of states and found that in the optical regime the corrections to the Dirac cone approximation are quite small [31]. Simsek generated a closed-form approximate expression based on Stauber's method, which generates results with less than 0.8% maximum absolute error for $\lambda > 250$ nm [32]. In this study, we first calculate the optical conductivity of graphene for the wavelength of $1.55 \mu\text{m}$ by following two different approaches developed by Gusynin *et al.* [27] and Stauber *et al.* [31], which are two most commonly used methods for the design and analysis of graphene devices. For the former, the scattering rate is assumed to be $\Gamma = 17$ K, Fermi velocity in graphene is taken as $v_F = 1.1 \times 10^6$ m/s [27]; for the latter 2.7 eV of hopping parameter is assumed [31]. Temperature is 300 K.

Fig. 10 shows the real and imaginary parts of σ_c as a function of chemical potential for $0 < \mu_c < 0.8$ eV. Results agree well with each other for the real part and there is a significant difference for the imaginary part around $\hbar\omega = 2\mu_c$, where \hbar is the reduced Planck constant, ω is angular frequency. The significant decrease observed in σ_i calculated by Stauber's method is due to the fact that it neglects any surface roughness. However, the difference is smaller in the region we are interested in, which is $0.45 < \mu_c < 0.55$ eV. The optical conductive of graphene can be converted into a complex electrical permittivity using $\epsilon_c = 1 - i\sigma_c/\omega\epsilon_0 d$, where d is the thickness of the graphene layer [34]. The complex refractive index can then be derived

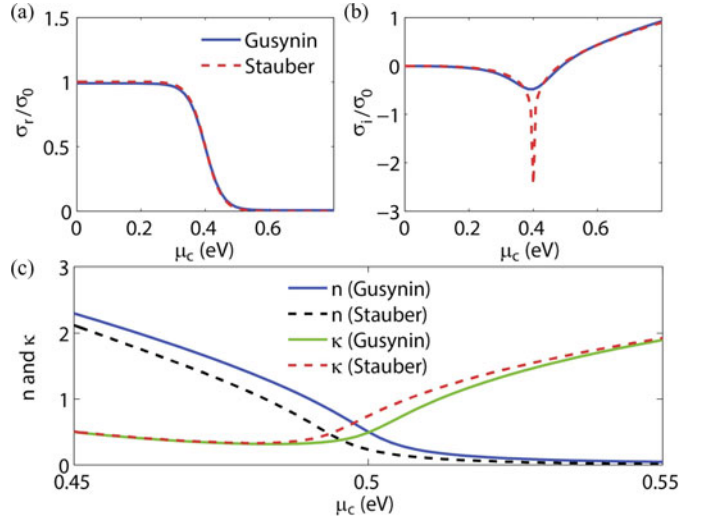


Fig. 10. (a) σ_r and (b) σ_i for $0 < \mu_c < 0.8$ eV at $\lambda = 1.55 \mu\text{m}$, normalized by $\sigma_0 = e^2/4\hbar$, where e is the unit charge. (c) Real (n) and imaginary (κ) parts of the refractive index of graphene calculated with two different approaches: solid lines [27], dashed lines [31] for $0.45 < \mu_c < 0.55$ eV at $\lambda = 1.55 \mu\text{m}$.

from ϵ_c . By following this procedure, we calculate the real and imaginary parts of the refractive index of graphene for $0.45 < \mu_c < 0.55$ eV and plot the results in Fig. 10(c). An interesting aspect about this region is when μ_c is changed from 0.49 to 0.5 eV, n slightly decreases while κ slightly increases becoming the dominating part. Using data from Fig. 10, we investigate the performance of GEOMs by replacing the ITO layer with a 0.7 nm thickness graphene film. The performance of the GEOM shows similar characteristics relative to the ITO-EOM from Fig. 6 (see Fig. 11). While these results are slightly inferior to the ITO case, they are still significantly superior to diffraction-limited devices [3], [4], [7]. Notice, the device length is only 0.78λ .

IV. ELECTRO-OPTIC PERFORMANCE

Here we provide a brief performance comparison of the ITO and graphene EOMs. The key performance figures of an EOM are the modulation efficiency (E/bit) and the bandwidth (i.e. speed), which can be optimized by varying different geometric parameters of the device discussed in Section II. Similarly, the modulator's ER and IL performance depends on the optical MOS mode, which can also be modified by altering the geometric parameters of the EOM as discussed above. Lastly, Table III provides a quantitative performance summary of ITO and graphene EOMs operating at $1.55 \mu\text{m}$ wavelength. Our EOMs can intrinsically work at an ultrahigh speed because of a sub-fF low capacitance. The operation speed is limited mainly by the RC delay. Here, we consider two different devices, which are $2 \mu\text{m}$ and $0.5 \mu\text{m}$ long, where t_{gate} and W_{Si} vary from 5 to 50 nm and 200 to 500 nm, respectively. The speed performance is estimated by calculating the RC delay time for the MOS capacitor with a resistive load of 50 to 500 Ohm.

Table III states two optimal device choices depending on the circuit design considerations for optimizing either the signal integrity or the data bandwidth, i.e., speed. As a general rule of

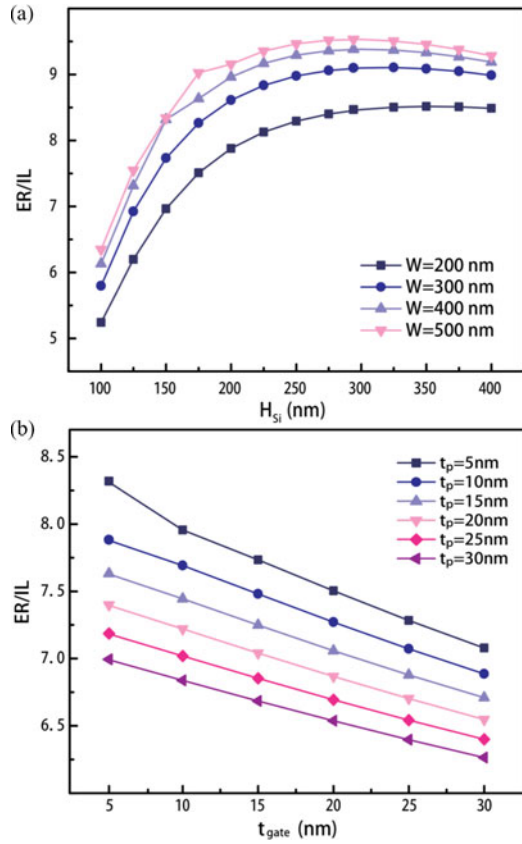


Fig. 11. Plasmonic graphene-based EOM performance. $t_{gate} = t_{passivation} = t_p = 5$ nm for silicon waveguide height and width study. $H_{ITO} = 10$ nm, $H_{Si} = 150$ nm and $W = 400$ nm for oxide layer study. $H_{Au} = 100$ nm for all the cases. The effective thickness of graphene is 0.7 nm, $\lambda = 1550$ nm.

TABLE III
QUANTITATIVE PERFORMANCE ANALYSIS

	ITO		Graphene	
	Signal	Speed	Signal	Speed
L				
Device Length - μm	2	0.5	2	0.5
R				
Resistance - Ohm		50 – 500		
C				
Capacitance - fF	0.94	0.23	2.64	0.66
BW				
Bandwidth - THz	21.2 – 2.1	84 – 8.4	7.5 – 0.7	30.2 – 3.0
IL				
Insertion Loss - dB	0.60	0.15	2.12	0.53
ER				
Extinction Ratio - dB	12	3	18	4
V				
Voltage - Volts	2-3	2-3	1-2	1-2
E/bit				
Energy per bit - fJ	1.88 – 4.25	0.47 – 1.06	1.32 – 5.29	0.33 – 1.32

Device is operating at the wavelength of 1.55 μm . The gate oxide thickness and width vary from 5 to 50 nm and 200 to 500 nm respectively. The bandwidth (BW) is calculated from $BW = 1/RC$ where R has values from 50 to 500 Ohm. Energy per bit (E/bit) is calculated by $E/bit = \frac{1}{2}CV^2$, where applied voltage is 1 to 2 V and 2 to 3 V for graphene and ITO respectively.

thumb, for high-speed applications require low RC delay times, resulting in short device lengths, while strong signal switching applications demand a longer device to achieve a high signal-to-noise ratio. From Table III, it is evident that a device length of 0.5 μm (ITO-EOM) offers a bandwidth of tens of THz with medium signal switching strength. However, a 2 μm -long device enables for a 12 dB strong data switching while maintaining THz modulation speeds. The energy per bit for all EOMs in Table III show a low switching energy ranging from 330 aJ to less than 5 fJ per bit. The calculation for the GEOM parallel those of the ITO case with a slight improvement in the modulation strength and operation speed while being comparable in power consumption.

V. CONCLUSION

In this paper we have analyzed an ultra-compact plasmonic ITO-EOM and GEOMs using SOI hybrid integration. Experimental results show that a 3λ long device features an extinction ratio and on-chip insertion loss of about 1 dB/ μm and 1 dB, respectively. We experimentally verified the EO switching capability and derived an index model for graphene for EOMs. Numerically simulating an optimized ITO-EOM, the insertion loss can be reduced to 0.25 dB while keeping ER at 6 dB/ μm . We also show an ultra-compact hybrid EOM that features a graphene MOS mode for enhanced light-matter interaction, which has great potential for designing next generation highly efficient EOMs. The estimated energy per bit for the ITO calculated is as low as 0.23 fJ for a bandwidth of 100 + THz with 2 V of applied voltage. GEOM energy per bit calculated in the paper is 0.17 fJ with a maximum bandwidth of ~ 58 THz with 1 V voltage applied. At the same time, this high modulation performance is accompanied by a reasonably low insertion loss of 0.03 and 0.06 dB for ITO and graphene, respectively.

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