Silicon MOSFETs – Novel materials and alternative concepts

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Introduction

- Transistor was first made at Bell Labs (fig1)
- New materials must be introduced in implementation of new CMOS generations (fig2)

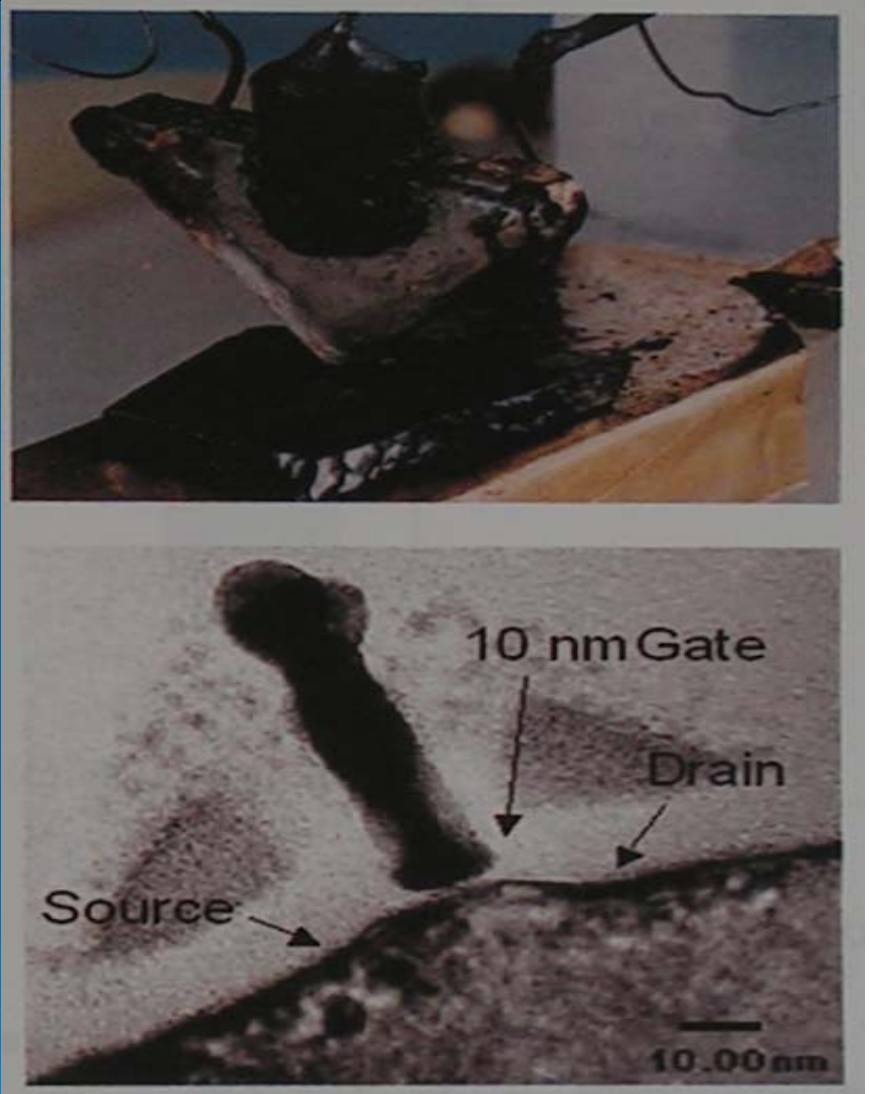


Figure 1: Photograph of the original point contact transistor in comparison with a TEM cross-section micrograph of a 10 nm gatelength research MOS-FET [2], [3].

Introduction

- Al has been replaced by Cu
- Cu interconnects are now embedded in low permittivity materials (low-K) like porous oxides

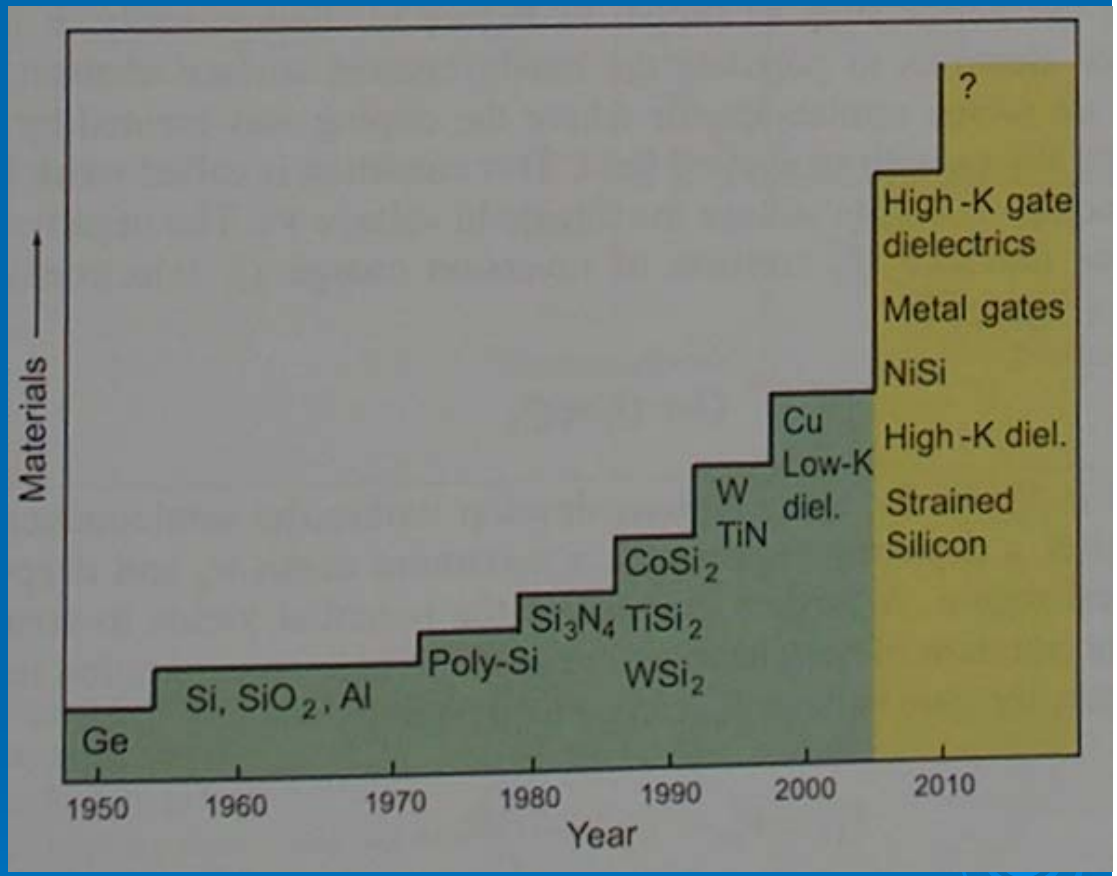


Figure 2: Implementation of new materials in CMOS processes [4].

Introduction

- **Various silicides** have been introduced as source, drain and gate contacts **to lower the device resistance**, TiSi2 has been replaced by CoSi2 which maintains lower resistance

- **High-K materials** will replace SiO2 gate insulator and metal gates will be used instead of Poly **to face the tunneling and gate leakage problems**

Introduction

- Following topics will be addressed:
  - Fundamentals of MOSFET devices
  - Scaling rules
  - Silicon dioxide based gate dielectrics
  - High-K materials for CMOS
  - Metal gates
  - Junctions and contacts
  - Advanced MOSFET concepts

Fundamentals of MOSFET devices

- MOS capacitor
  - Figure (fig3) shows the structure of a MOS capacitor
  - The corresponding band diagram is shown in figure (fig4)
  - Silicon dioxide has a 9 eV bandgap
  - This results in large band offset relative to silicon

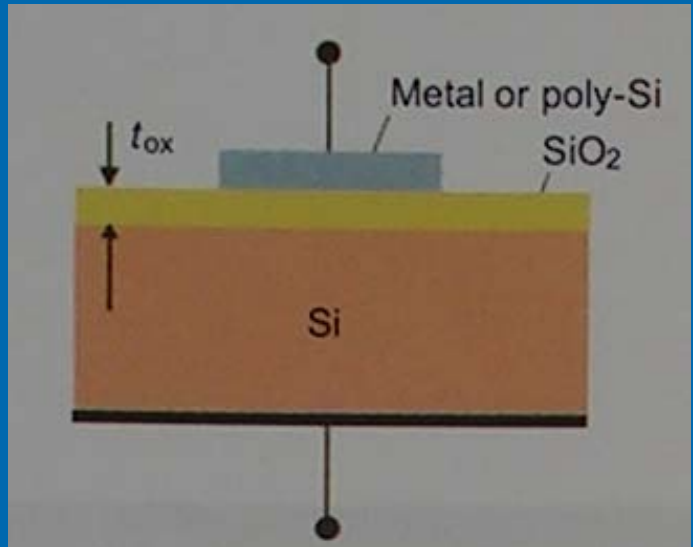


Figure 3: Schematic structure of a MOS capacitor.

Fundamentals of MOSFET devices

- Potential barrier between conduction band of silicon and silicon dioxide is large (3.2 eV)
- This controls charge transport through dielectric layer

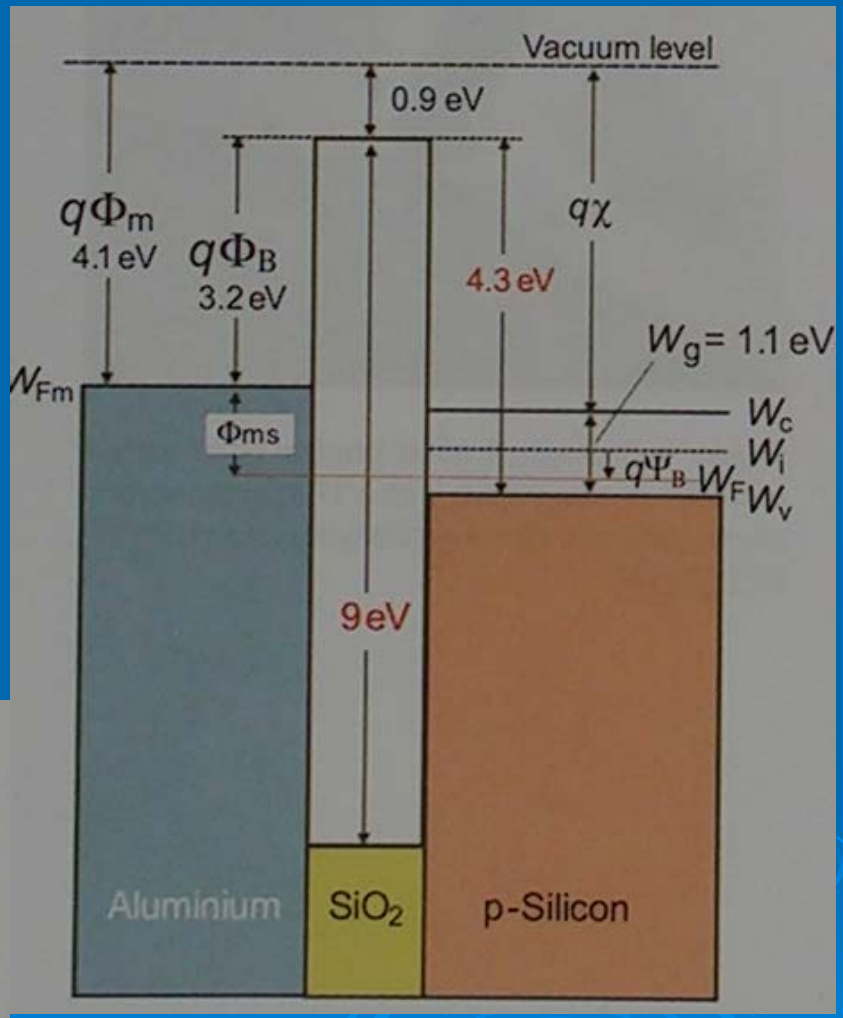


Figure 4: Energy-band diagram of the three components of a real MOS capacitor, consisting of an Al contact, silicon dioxide and p-type silicon. $q\Phi_m$ denotes the work function of the metal, $q\Phi_{ms}$ the workfunction difference of Al versus p-Si, χ the electron affinity of the silicon, W_g the band energy, W_c the conduction band, W_v the valence band of silicon, $q\Psi_B$ the difference between the intrinsic Fermi level W_i and the Fermi level W_F [5].

Fundamentals of MOSFET devices

- Energy band diagram of an ideal MOS capacitor with a p-type semiconductor is shown in figure (fig 5)

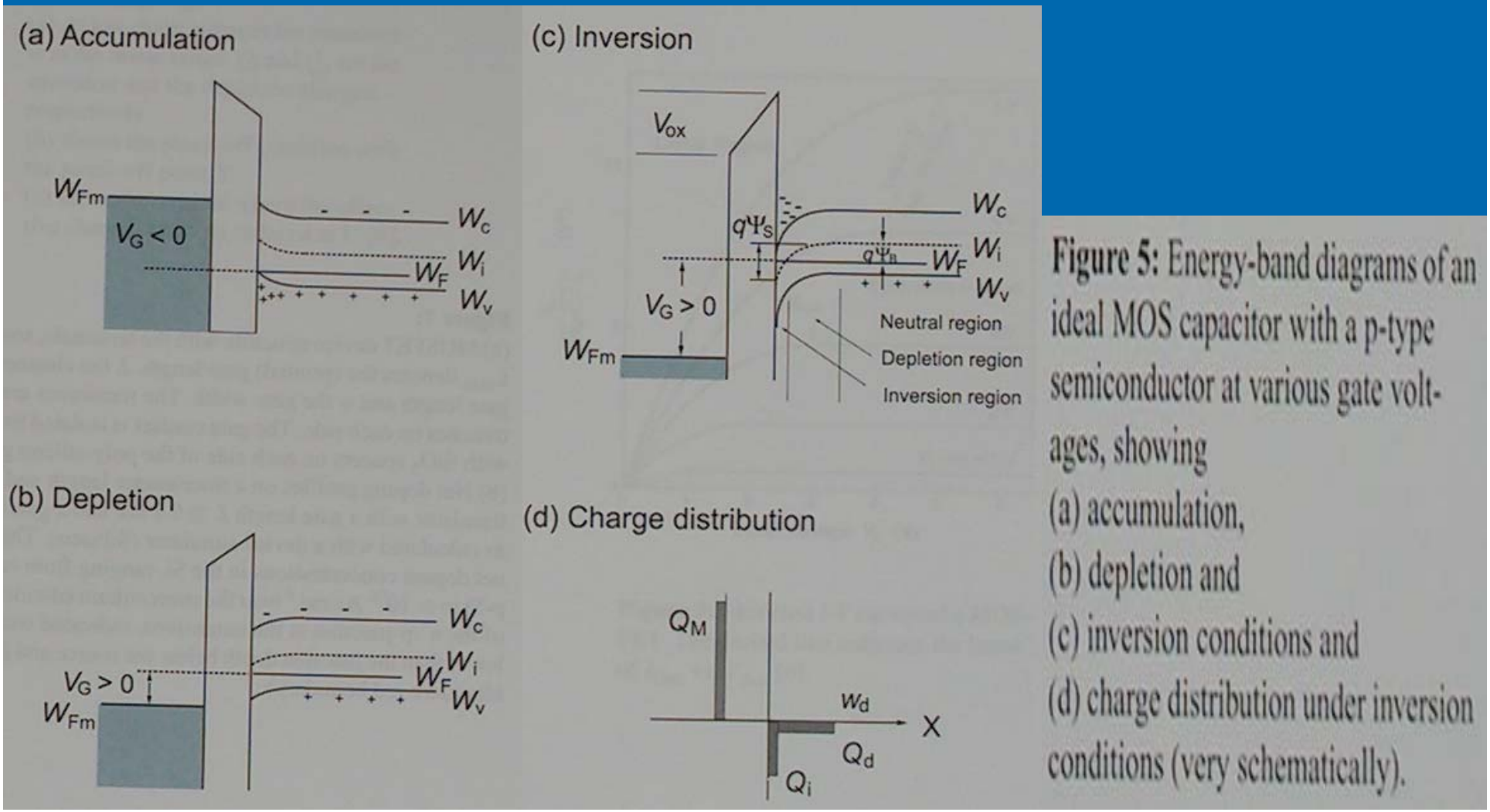


Figure 5: Energy-band diagrams of an ideal MOS capacitor with a p-type semiconductor at various gate voltages, showing
(a) accumulation,
(b) depletion and
(c) inversion conditions and
(d) charge distribution under inversion conditions (very schematically).

Fundamentals of MOSFET devices

- VG < 0 :
  - Fermi level of metal increases, an electric field is created in Sio2 (slope of the conduction band of SiO2)
  - Due to low carrier concentrations, Si bands bend at the interface of SiO2, leading to ***accumulation*** of excess hole
  - To conserve charge, equivalent number of electrons is accumulated at metal side

Fundamentals of MOSFET devices

- VG>0:
  - Fermi level moves down, silicon bands bend downward
  - Hole concentration near the interface decreases
  - This is called ***depletion*** condition
  - Equivalent amount of positive charge will be induced at the metal oxide interface QM as negative charge in semiconductor Qs : Q = -QM , Qs = Qd

Fundamentals of MOSFET devices

- Qd originates from ionized donor states
- A further increase of the positive gate potential enhances band bending
- At a certain gate potential the intrinsic Fermi level crosses the Fermi level as shown in Figure c
- Electrons now populate the newly created surface channel
- Surface behaves like an n-type semiconductor
- This is called ***weak Inversion***

Fundamentals of MOSFET devices

- The corresponding gate voltage is called threshold voltage V_T
- Negative charge at semiconductor interface consists of inversion charge Qi and ionized acceptors Qd : Q = Qi + Qd
- Three regions are developed in the semiconductor (fig C):
  - Inversion region
  - Depletion region (maximum depth Wd)
  - Neutral region

Fundamentals of MOSFET devices

- Further increase in VG results in ***Strong Inversion***
- Concentration of electrons exceeds the hole concentration (Qi>Qd)
- Gate voltage can be expressed as

$$V_G = V_{ox} + \psi_S = \frac{-Q_s}{C_{ox}} + \psi_S$$

  - Cox is oxide capacitance per unit area
  - Ψs is the surface potential
  - Qs and Ψs can be obtained by **solving Poisson equation** with appropriate boundary conditions
  - Under extreme accumulation and inversion, VG and Vox are much larger than Ψs, then :

$$Q = -C_{ox}V_G, \; Cox = \frac{\varepsilon_{ox}}{t_{ox}}$$

Fundamentals of MOSFET devices

- Total capacitance of MOS capacitor is a series combination of oxide capacitance Cox and the semiconductor capacitance Cs
- Figure shows C-V curve for an ideal MOS capacitor (fig6)

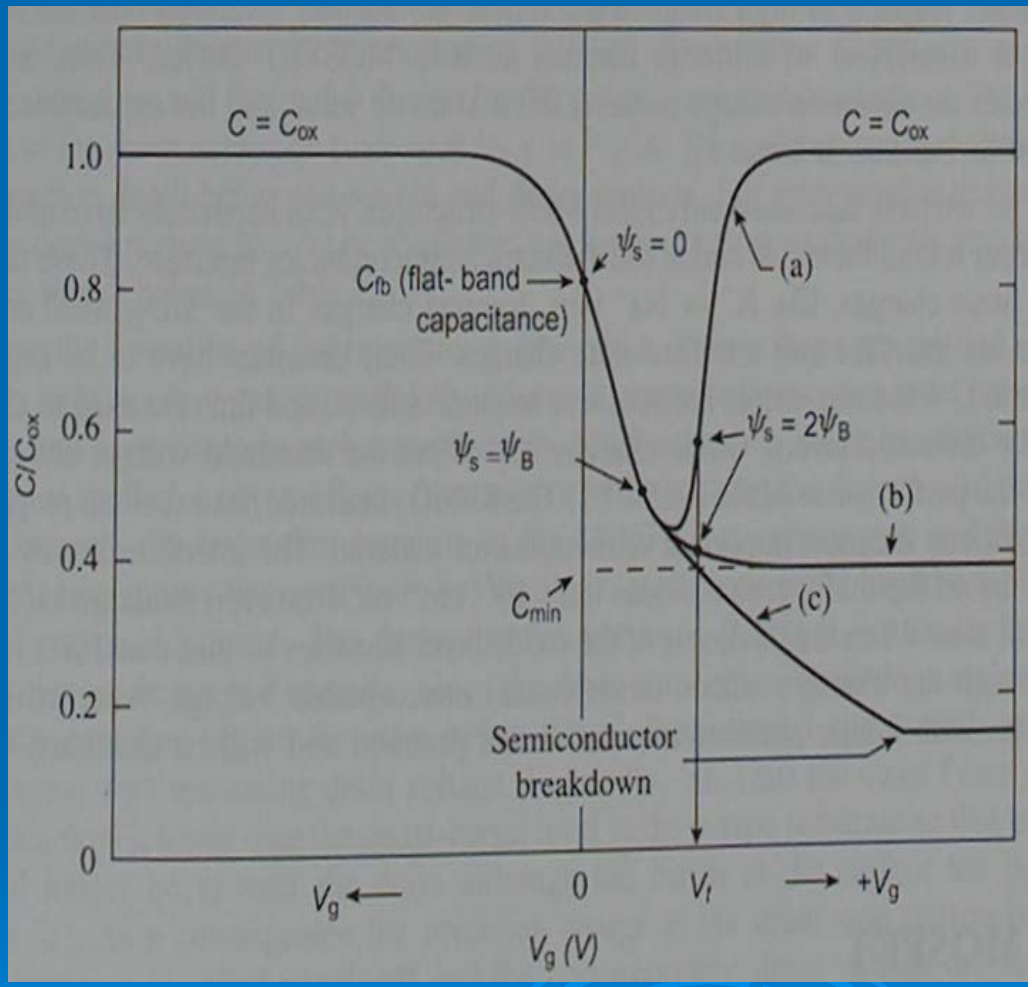


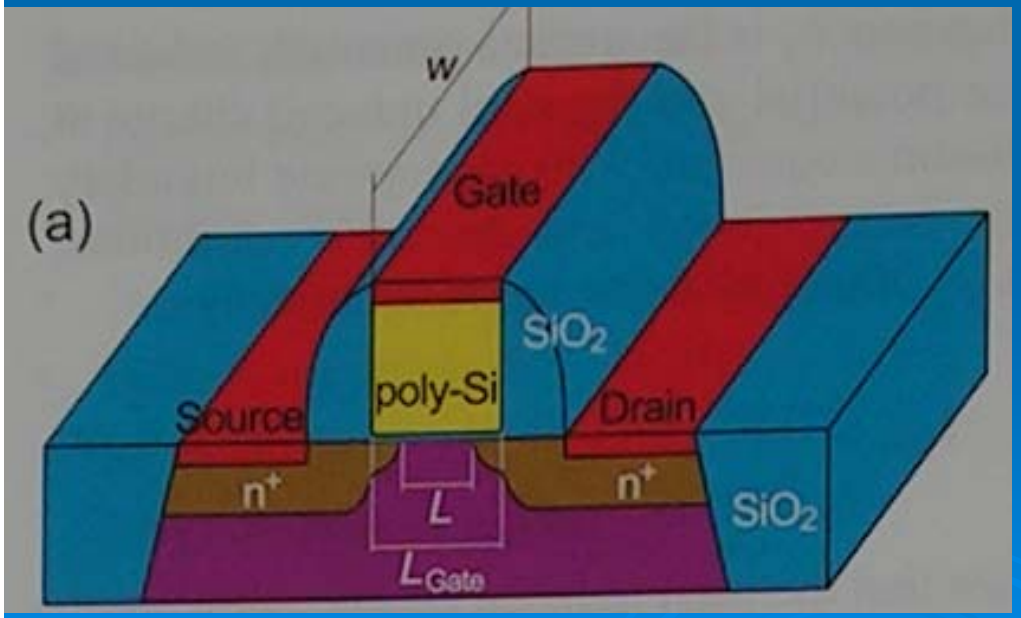
Figure 6: *C-V* curve of an ideal MOS capacitor under
(a) low frequency,
(b) high frequency and
(c) deep-depletion conditions [6].

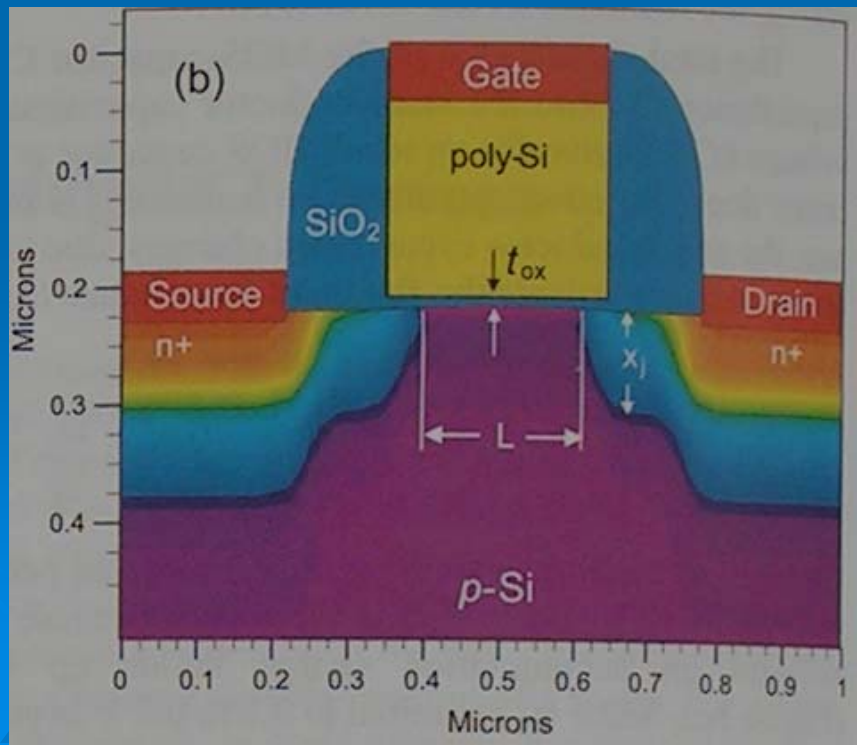
Fundamentals of MOSFET devices

- Cox is independent of voltage, Cs changes due to different charge states discussed

➢ MOSFET

- Figure shows basic MOSFET structure (fig 7)





Fundamentals of MOSFET devices

- Substrate is p-type and source and drain are n+-doped
- A sufficiently large gate potential VG induces a conducting inversion layer between the source and drain, similar to MOS capacitor
- The additional drain voltage causes a current to flow from source to drain

Fundamentals of MOSFET devices

- Figure (fig 8) illustrates the operation of MOSFET at various gate and drain voltages

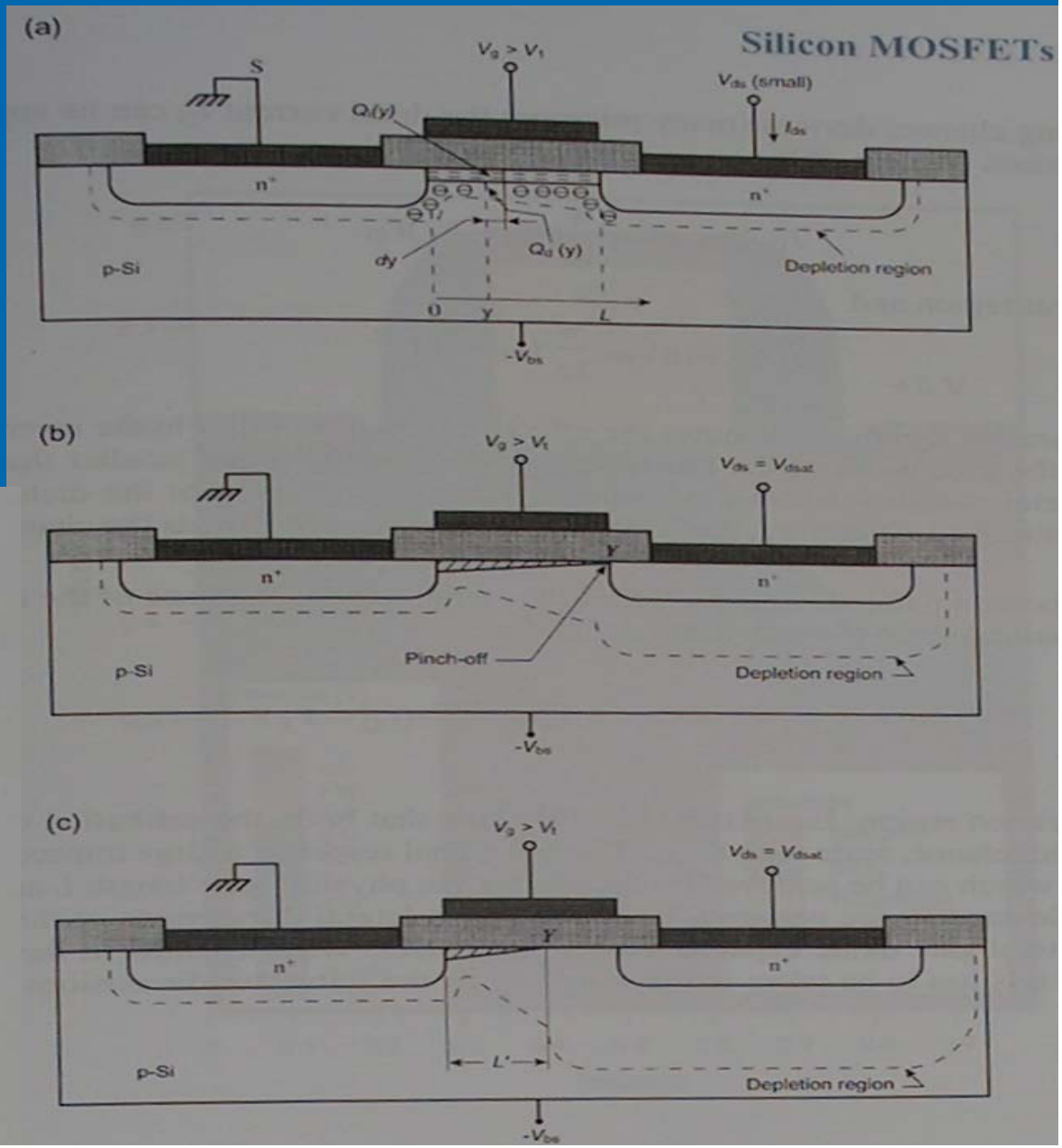


Figure 8: MOSFET operation at a gate voltage $V_g > V_t$ with increasing drain voltage V_{ds}.
(a) At low drain voltages the transistor is in the linear range. Q_i and Q_d are the inversion and the depletion charges, respectively.
(b) shows the pinch-off condition with the pinch-off point Y.
(c) saturation regime where the effective channel length is reduced to L' [6].

Fundamentals of MOSFET devices

- At low drain voltages (fig a) the drain current increases linearly as shown in Figure (fig 9)
- Drain-substrate n+-p diode is under reverse bias and depletion region increases as drain voltage is increased , it extends under gate region
- Inversion can no longer occur at drain, inversion charge at drain side approaches zero
- This condition is called **pinch-off** and the corresponding drain voltage **saturation voltage**
- Channel resistance increases, channel current is saturated

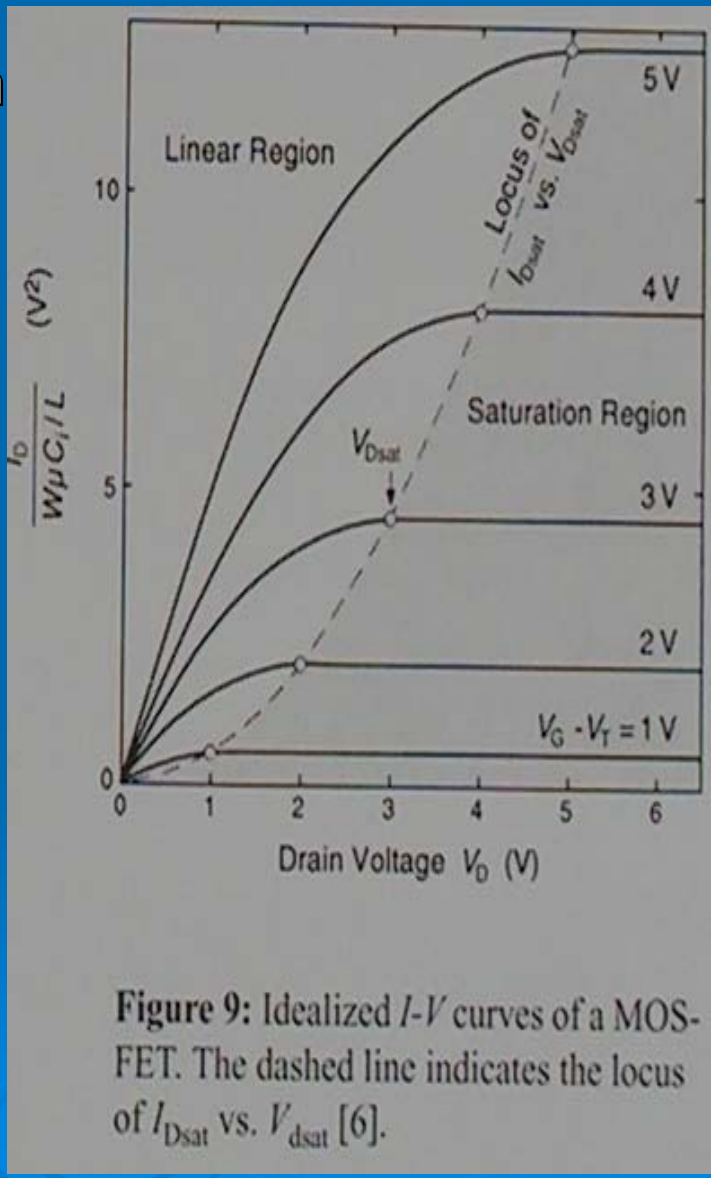


Figure 9: Idealized *I-V* curves of a MOSFET. The dashed line indicates the locus of I_{Dsat} vs. V_{dsat} [6].

Fundamentals of MOSFET devices

- For long channel devices the drain current can be approximated:

$$\text{for linear region}: I_D \cong \mu_{eff} C_{ox} \frac{w}{L}(V_G - V_T)V_D$$

$$\text{for saturation region}: I_D \cong \mu_{eff} C_{ox} \frac{w}{2L}(V_G - V_T)^2$$

$$\mu_{eff}: \text{effective carrier mobility, w}: \text{gate width of transistor}$$

- Transconductance, g, per unit width is defined as:

$$g = \frac{1}{w}\frac{\partial I_D}{\partial V_G}\Big|_{V_D = const} = 2\mu_{eff}\frac{Cox}{L}(V_G - V_T)$$

- Both saturation current and transconductance scale with Cox/L
- As lateral dimensions of the transistor shrink, the total gate oxide capacitance decreases

Fundamentals of MOSFET devices

- When the gate length of MOSFET is reduced to submicron dimensions, the electric field distribution in the channel region is transformed from one dimensional to 2-D
- In long gate devices, potential contours are parallel to oxide/silicon interface
- For short channel devices, drain voltage generates a 2-D potential distribution

Fundamentals of MOSFET devices

- Figure (fig 10) illustrates potential contours for a short channel device

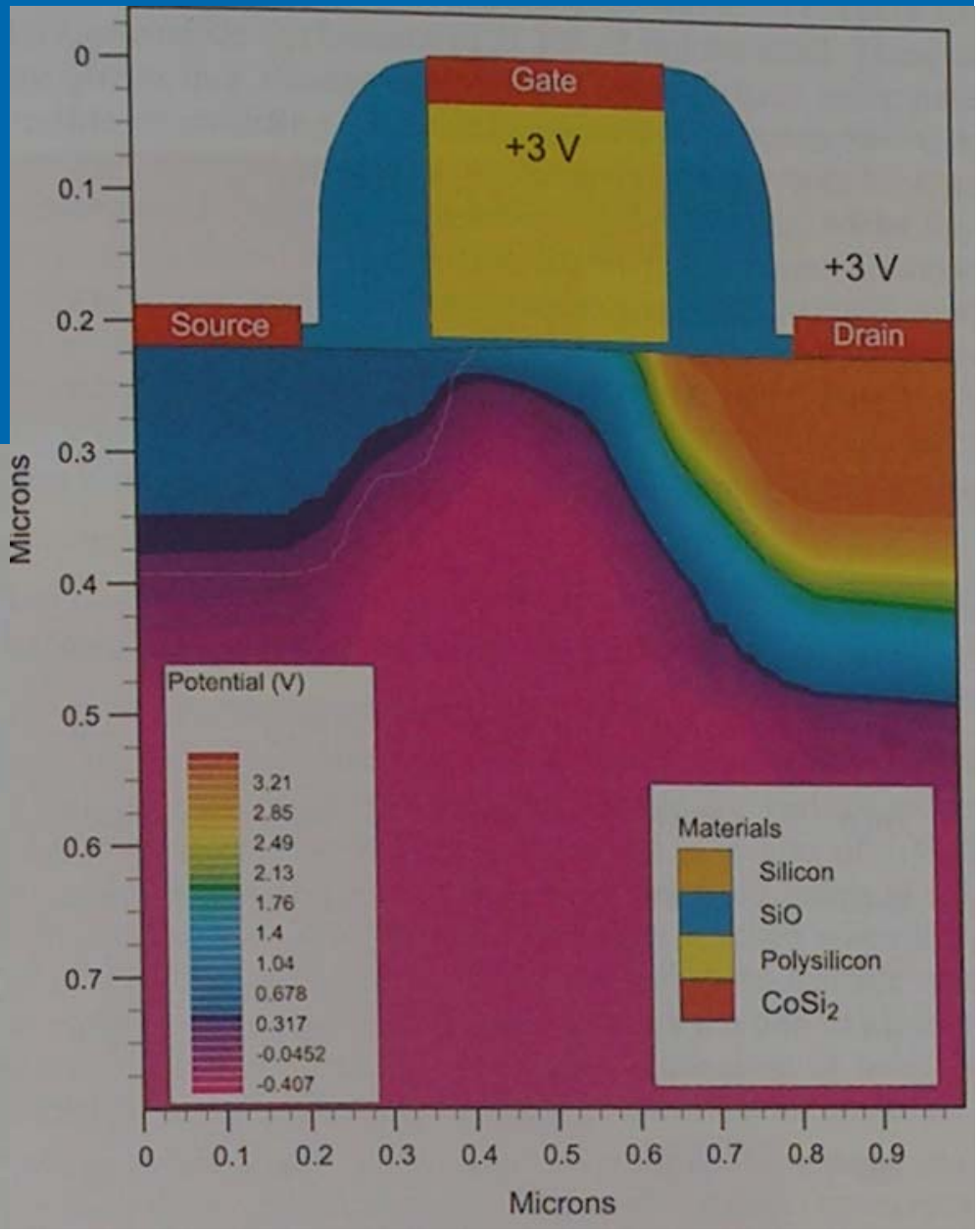


Figure 10: Simulated potential distribution of a 0.2 μm MOSFET with $V_G = 3$ V and $V_D = 3$ V. Near the drain region the potential lines are strongly affected by the drain voltage. The thin solid line indicates the n+/p-junctions.

Fundamentals of MOSFET devices

- Therefore, small transistors tend to exhibit undesired effects:
  - Lack of saturation
  - Gate oxide degradation due to hot electrons
  - Threshold voltage shifts
  - Gate-induced drain leakage
  - Drain induced barrier lowering, lowering potential barrier at the source channel side with increasing drain voltage

Scaling Rules

- Simplest scaling concept for MOSFETs is **constant-field scaling :**
- Scale device dimensions as well as voltages by the same factor α, proportionally increase substrate doping to keep the electric field pattern unchanged

- This implies that oxide thickness has to be reduced to maintain the oxide field while decreasing the gate voltage

Scaling Rules

- Table shows constant field scaling on different parameters (table 1)

	MOSFET device and Circuit Parameters	Multiplicative Factor ($\alpha > 1$)
Scaling assumptions	Device dimensions (t_{ox}, L, w, x_j)	$1/\alpha$
	Doping concentration (N_a, N_d)	α
	Voltage (V_D)	$1/\alpha$
Derived scaling Behavior of device Parameters	Electric field (E)	1
	Depletion-layer width (w_d)	$1/\alpha$
	Capacitance ($C = \varepsilon A/t_{ox}$)	$1/\alpha$
	Inversion-layer charge density (Q_i)	1
	Carrier velocity	1
	Current, drift (I)	$1/\alpha$
Derived scaling Behaviour of device Parameters	Circuit delay time ($\tau \sim CV_D/I_D$)	$1/\alpha$
	Power dissipation per circuit ($P \sim V_D I_D$)	$1/\alpha^2$
	Power-delay product per circuit ($P\tau$)	$1/\alpha^3$
	Circuit density ($\propto 1/A$)	α^2
	Power density (P/A)	1

Table 1: Device and circuit parameters resulting from constant field scaling [6].

Scaling Rules

- Based on this, circuit delay time decreases by a factor of α and power dissipation by α^2
- Advanced scaling models can be found in references
- Scaling requires an ever-increasing specific capacitance in the channel
- This has been done by **reducing oxide thickness**
- Use of thinner silicon dioxide gates is limited by the exploding gate leakage as shown in figure (fig 11)

Scaling Rules

- Use of high-K dielectrics is anticipated
- High-K oxide thickness is usually converted into Sio2 Equivalent Oxide Thickness (EOT)

$$t_{eq} = \frac{\varepsilon_{SiO2}}{\varepsilon_{film}} t_x$$

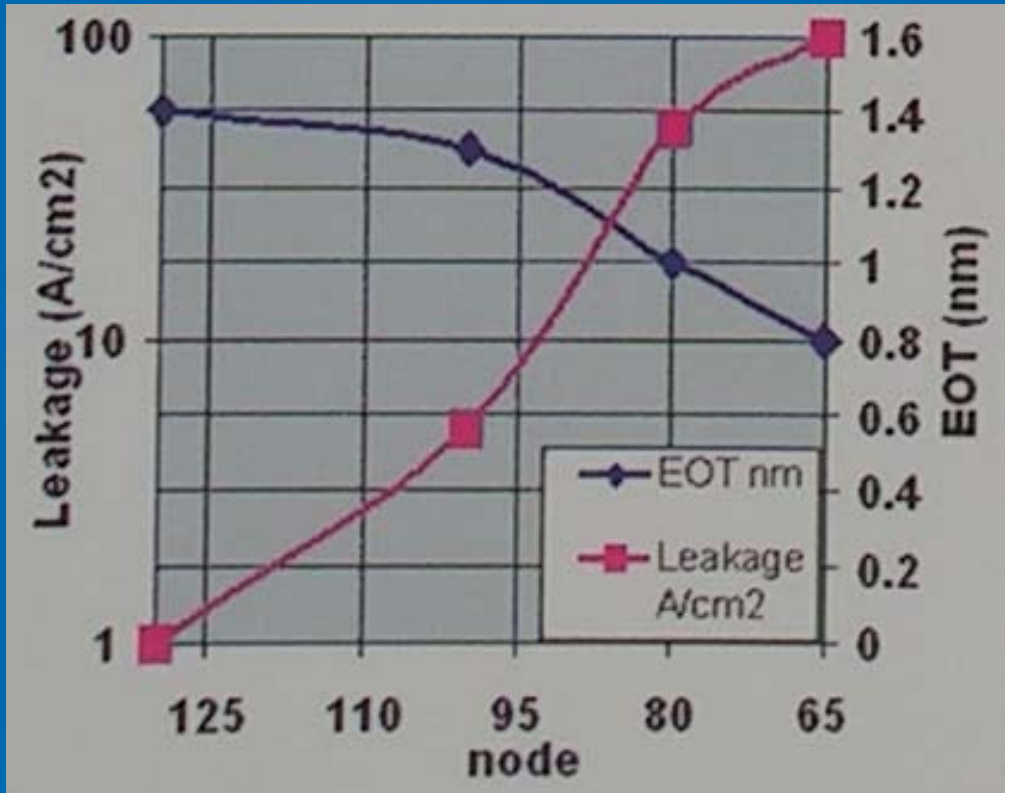


Figure 11: Gate leakage current and equivalent oxide thickness (EOT) versus technology node given in nm.

Silicon-Dioxide Based Gate Dielectrics

- Today's main stream MOSFETs gate oxide thickness of 1.5-2 nm
- Thinning down the oxide raises severe technological problems:
  - Dielectric thickness variation
  - Penetration of impurities, particularly boron, from the highly doped polysilicon gate
  - Reliability and lifetime problems for devices
  - Gate leakage current

Silicon-Dioxide Based Gate Dielectrics

- Figure (fig13) demonstrates the gate leakage problem

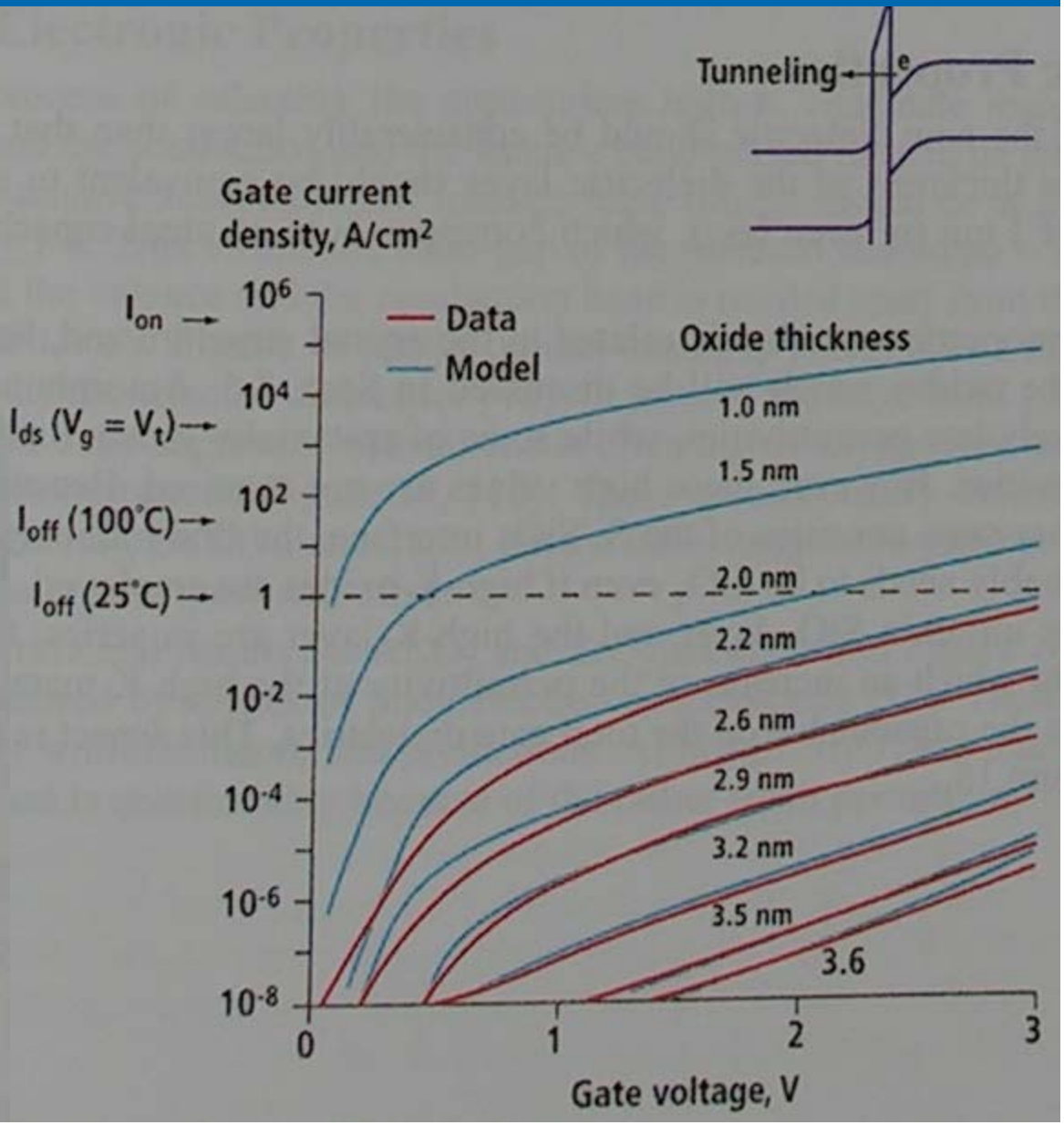


Figure 13: Measured (red curves) and simulated (blue lines) gate leakage current versus gate voltage for various oxide thicknesses. The leakage current increases exponentially as the oxide thickness is scaled down. The inset illustrates direct tunneling through the oxide [8].

Silicon-Dioxide Based Gate Dielectrics

- For low power applications gate leakage current reduces battery life in stand-by mode
- Numerous attempts to improve oxide quality
- Introducing nitrogen to SiO2 leads to formation of SiO_xN_y **(Oxynitrides)**
- Nitrogen improves interface uniformity and reduces boron penetration and makes the oxide less sensitive to hot electrons

Silicon-Dioxide Based Gate Dielectrics

- Too much nitrogen at the silicon interface degrades carrier mobility and transconductance
- Nitrided silicon oxide reduces leakage current by one to two order of magnitude

High-K materials for CMOS

- High-K materials can solve the leakage current problem of Silicon dioxide
- Table give a list of potential high-K materials
- New dielectrics must fulfill a number of requirements that will be discussed in the following

Silicon-Dioxide Based Gate Dielectrics

- Dielectric properties
  - Permittivity should be considerably higher than SiO_2
  - Because of the superior low interface state densities of Si/SiO_2 the first monolayer of dielectric needs to be SiO_2
- Thermodynamics
  - The sandwich of gate, gate oxide and silicon is subjected to severe temperature changes
  - No chemical reactions are allowed
- Electronic properties
  - Bandgap energy and conduction and valence band offsets have o be taken into account
  - these offsets have to be at least 1 eV to achieve low leakage
  - Band gap of material must be > 3.1 eV

Silicon-Dioxide Based Gate Dielectrics

- High-K deposition tools and chemistry
  - An adequate deposition technology must be made available to semiconductor industry for the selected high-K material
  - Four deposition mechanisms can be considered:
    - Evaporation
    - Sputter deposition
    - Chemical vapor deposition
    - Atomic layer deposition

Silicon-Dioxide Based Gate Dielectrics

- Metal organic chemical vapor deposition (MOCVD) and atomic layer deposition are attractive for high-k materials

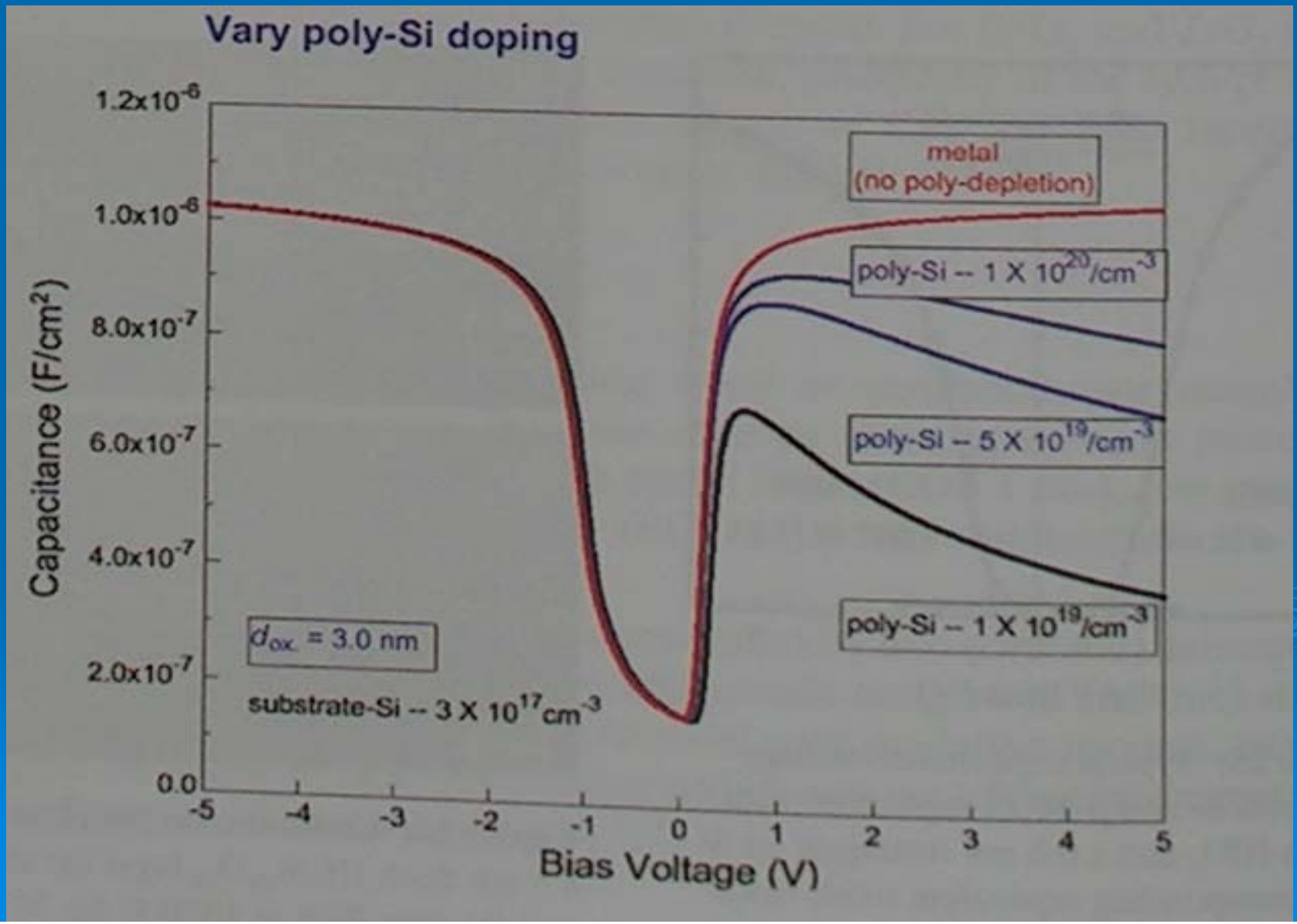
- Process compatibility
  - High-k gate etch
  - System on a chip : different gate oxide processes are required for different parts of the chip
- Microstructural stability
  - Structure should be stable through processing

Metal Gates

- Polysilicon vs. metal gates
  - Standard CMOS uses heavy doped poly-silicon as gate
  - Its work function can be adjusted by doping for p and n devices
  - Disadvantage: high resistivity, formation of a depletion layer
  - Depletion requires use of thinner gate oxides
  - Resistivity limits the current drive
  - Use of metal gates relaxes requirements of high-K dielectrics

Metal Gates

- Figure (fig 29) shows C-V curves for a poly-si gate



Metal Gates

- Metal gate material selection
  - Similar to high-K oxide materials, metals gates must have these properties:
    - Thermodynamic stability
    - electronic properties
    - Process compatibility
  - Different metals are needed for gates of PMOS and NMOS (to obtain suitable band alignment)
  - for NMOS the only metals wit sufficiently high melting point are Ti, Ta, Nb

Metal Gates

- Co, Re, Ni and Ru may be considered for PMOS
- High melting metallic alloys are also potential candidates
- Integration of dual metal gates in standard CMOS is difficult
- Fully depleted silicon on insulator (SOI) MOSFETs require just one metal gate
- Performance advantages of SOI devices make them very attractive

Junctions and contacts

- Shallow junctions
  - Series resistivity of MOSFET associated with contacts, shallow junctions and channel are illustrated in the figure (fig 32)
  - Drive capability is limited by these resistances

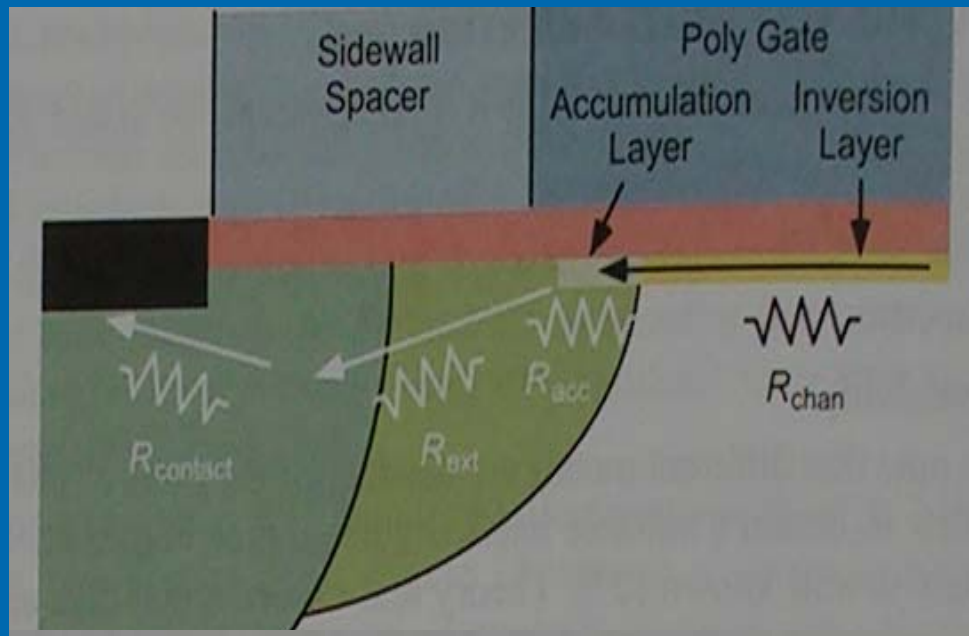


Figure 32: Schematic cross section of the source/channel boundary and part of the channel region. Arrows indicate the current flow path and the resistors illustrate the various regions that can affect the current drive capability of the device.

Junctions and contacts

- Channel resistance: $R_{chan} = [\frac{w}{L} \mu \frac{\varepsilon_{ox}}{t_{ox}} (V_G - V_T)]^{-1}$
- Total other resistances must be less than 10% of channel resistance
- Channel resistance would remain constant as technology scale (ideal scaling)
- In this case, parasitic resistance need to remain constant in different generations
- This will be difficult as doping concentrations will become limited
- Shallow junctions are proposed to alleviate some of the problems

Junctions and contacts

- Junction contacts
  - Another major resistance component in a device
  - Normally made by silicides contacting heavily doped silicon
  - Contact resistance depends on the effective area of the contact
  - Approximate contact resistance is 1000 ohms
  - To keep this constant, contact resistivity must scale directly with contact area

Junctions and contacts

- Beyond 100 nm, the required resistivities are not achievable by current contact mechanisms
- Contact resistivity:

$$\rho_c = \rho_{c0} \exp\left[\frac{2\sqrt{\varepsilon_s m^*}}{\hbar} \frac{\phi_B}{\sqrt{C_s}}\right]$$

- Depends on Cs : dopand solubility in silicon and φB : barriers height

Advanced MOSFET concepts

- Research MOSFETs with gate lengths of 10 to 15 nm have been fabricated
- Undesired short channel effects will become dominant
- Alternative transistor concepts must be employed to reduce these effects
- SOI substrates are promising
- SOI transistors have smaller parasitic capacitors, smaller leakage, immune to soft errors, higher speed and lower power consumption

Advanced MOSFET concepts

- SOI substrate is more expensive and may have heat transfer problems
- Figure (fig 36) shows different approaches

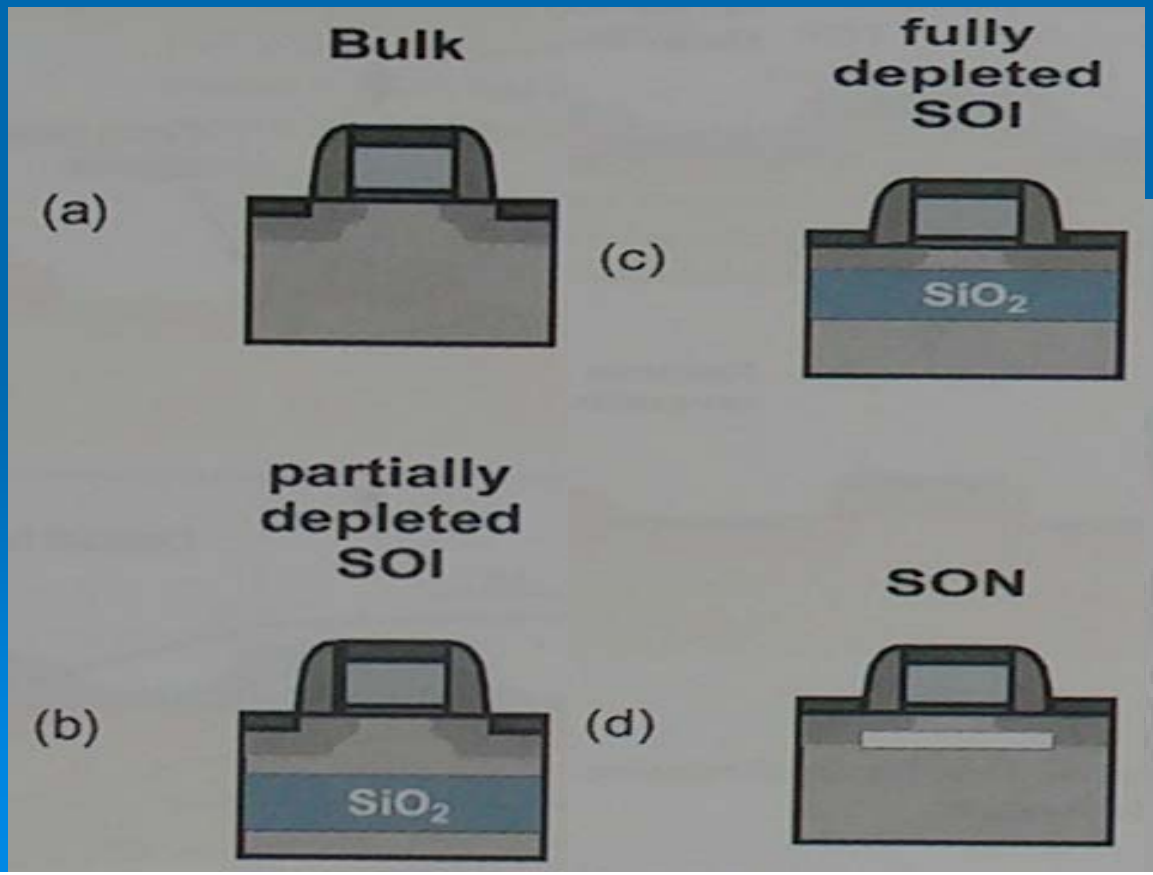


Figure 36: Conventional bulk MOSFET (a) compared with SOI (b, c) and SON-Transistor concepts (d).

Advanced MOSFET concepts

- Ultra-thin body (UTB) transistors can be made on SOI
  - Si body has a thickness less than 10 nm
- Double-gate transistors (DG) are investigated (fig38)

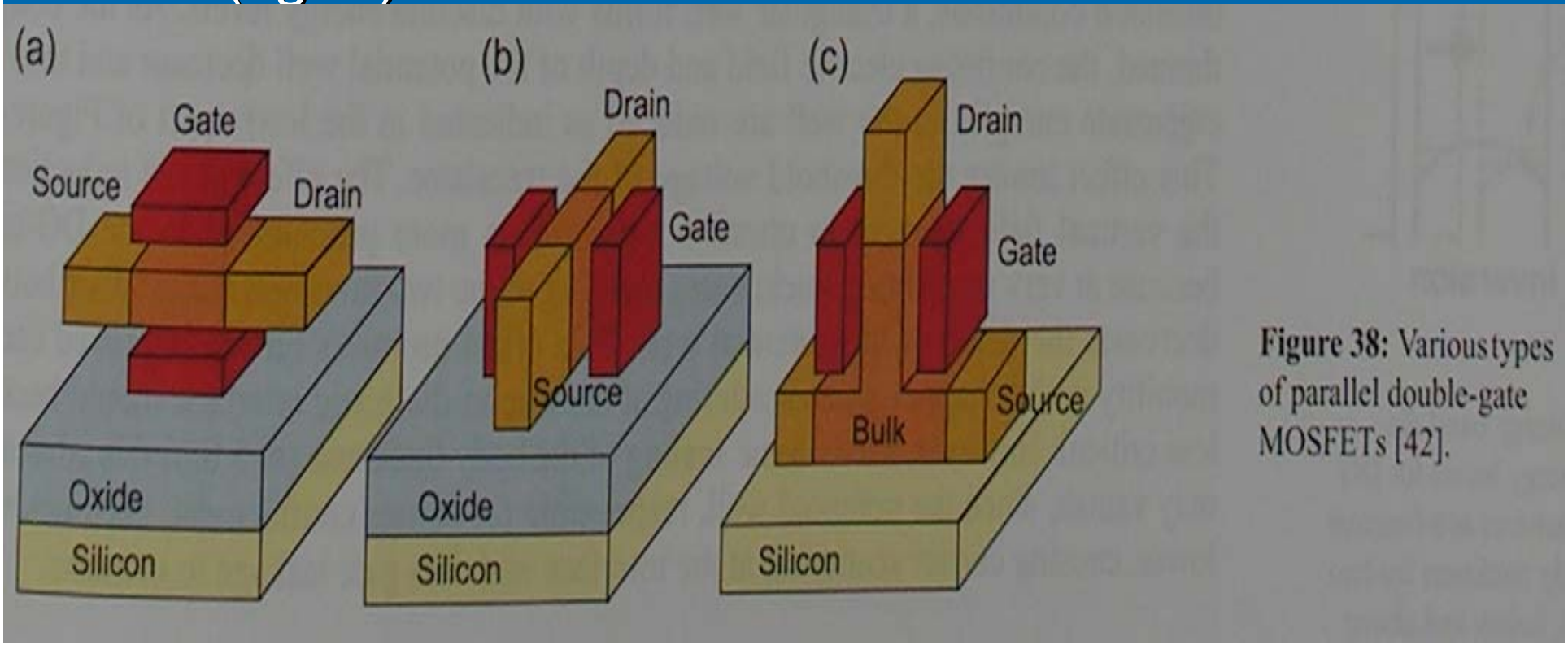


Figure 38: Various types of parallel double-gate MOSFETs [42].

Advanced MOSFET concepts

- In vertical DG, gate length can be determined by ion implantation and diffusion and not lithography
- DG transistors are very difficult to fabricate

- Both DG and UTB rely on thickness of silicon channel to control short channel effects and minimize leakage
- Another possibility for improving device performance is use of **strained silicon** and strained $Si_{1-x}Ge_x$ layers