UMBC CMPE 212, Spring 2023

Lab 7 addendum

In the last Lab, you simultaneously minimized the switching expressions for all 7 signals needed to drive a 7-segment display.

Implement each of those switching expressions using AND, OR and NOT gates in structural Verilog;
assuming that maximum fan-in of a gate (i.e., the maximum number of inputs that a/any gate can have is limited to 4).

Then simulate your 7-segment display in Verilog and show the printouts to the TA.

Do you see any difference between the version where you assumed don't cares (for inputs corresponding to decimal numbers 10 thru 15) and the version where there are no don't cares (because you display hex digits A thru F corresponding to the inputs 10 thru 15) ??