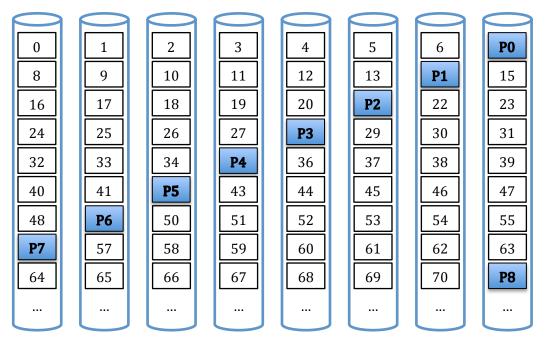
CMSC611: Advanced Computer Architecture Homework 6 Solutions

Question 1:

(50 points)

a) The layout of blocks across disks of the RAID 5 system is like:



b) In order to perform reconstruction, the RAID 5 system needs to read the data or parity blocks from 7 working disks and write the data or parity block to the fail disk. If failures are independent for the eight disks, the expected time until a reconstruction can be estimated based on the MTTF for each disk:

Expected Time =
$$\frac{\text{MTTF}}{\text{Number of disks}} = \frac{3 \times 10^6 \text{ hours}}{8} = 375,000 \text{ hours}$$

c) With the peak sequential read rate, each disk can read 400MB/sec. Consider all reads are parallel,

Read Time =
$$\frac{\text{Disk capacity}}{\text{Read rate}} = \frac{100\text{GB}}{400\text{MB/sec}} = 250\text{s}$$

With the peak sequential write rate, each disk can write 200MB/sec, so

Write Time =
$$\frac{\text{Disk capacity}}{\text{Write rate}} = \frac{100\text{GB}}{200\text{MB/sec}} = 500\text{s}$$

Write can only occur after all reads are completed, so the minimum offline reconstruction time is

 $\text{Reconstruction}_{\text{offline}} = \text{Read time} + \text{Write time} = 250 + 500 = 750\text{s}$

d) Considering the 40MB/sec limitation, the rate of each disk for the read or write is

Read/Write Rate =
$$\frac{\text{Total bandwidth}}{\text{Number of disks}} = \frac{40\text{MB/sec}}{8} = 5 \text{ MB/sec}$$

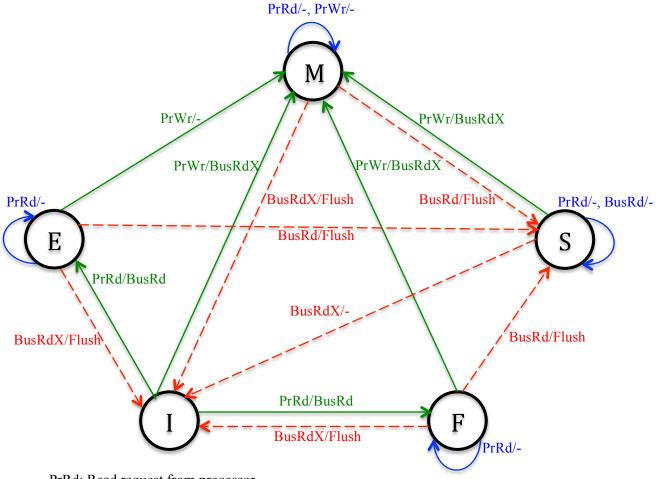
If all read and write operations can be parallel, the online reconstruction time is

Reconstruction_{online} =
$$\frac{\text{Disk capacity}}{\text{Read/Write rate}} = \frac{100\text{GB}}{5\text{MB/sec}} = 20,000\text{s}$$

Question 2:

(50 points)

a) The MESIF state transition diagram is shown as the following:



PrRd: Read request from processor PrWr: Write request from processor BusRd: Read request from the bus without intent to modify BusRdX: Read request from the bus with intent to modify The transitions are labeled as "action observed/action performed".

b)					
Processor 1	Processor 2	MESIF State		Transition	Bus
		P1	P2		Message
Read address A		Е		PrRd	BusRd
	Read address A		F	PrRd	BusRd
		S		BusRd	Flush
Read address A		S		PrRd	-
	Write to address A		М	PrWr	BusRdX
		Ι		BusRdX	-
Read address A		F		PrRd	BusRd
			S	BusRd	Flush
Read address B		I(A)		PrReplace(A)	-
		F(B)/ E(B)		PrRd(B)	BusRd(B)
	Read address A		S	BusRd	-
	Write to address A		М	PrWr	BusRdX