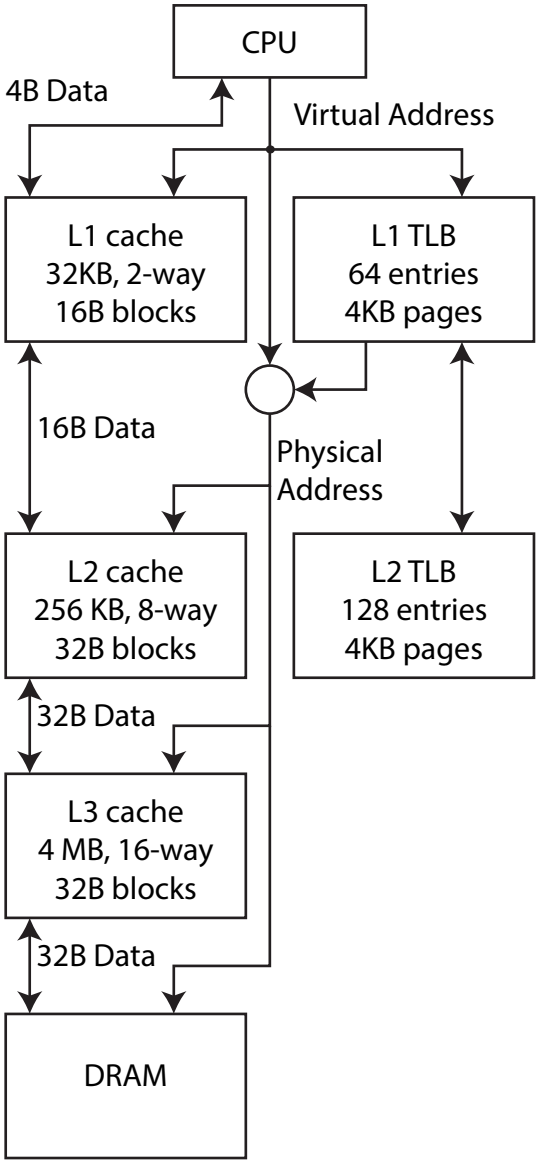
CMSC611: Advanced Computer Architecture
Homework 5

Question 1: (70 points)

Consider a CPU with three levels of cache, and two levels of TLB.

- The L1 cache uses virtual addresses and has a 1-cycle hit time
- The L2 cache uses physical addresses, and has a 5-cycle hit time.
- The L3 cache also uses physical addresses, and has a 15-cycle hit time.
- Memory has a 100-cycle access time.
- The L1 TLB is fully associative. The TLB check is started at the same time as the L1 cache check, but takes 4 cycles to complete.
- The L2 TLB is also fully associative, and takes 10 cycles to complete.

The system layout is as shown on the left, and the initial L1 and L2 TLB contents are as shown on the right:



L1 TLB:

Virtual Page	Physical Page
2F556	D217E
E225B	0C28C
037F8	D1E1B
…	…
8F9AB	B4F2F

L2 TLB:

Virtual Page	Physical Page
037F8	D1E1B
2B76C	CCBF2
2F556	D217E
7D6DF	124A5
8F9AB	B4F2F
124A5	036B0
E225B	0C28C
…	…
F3D2B	DCB8B

If the CPU reads a word at virtual address 2F556BE0, which is in L2 cache and has an entry in the L1 TLB, but is not L1 cache, the sequence of operations would be:

Clock	Action
0	CPU→L1 cache: look up 4 bytes at tag BD55, index 2BE, offset 0 (miss) CPU→TLB: look up virtual page 2F556
…	
3	TLB returns translation to physical page D217E Construct physical address D217EBE0
4	L1→L2 cache: look up 16 bytes at tag 1A42F, index 35F, offset 0
…	
8	L2 returns data for physical addresses D217EBE0–D217EBEF L1 replaces one block in set at index 2BE, tag BD55 CPU gets data for virtual address 2F556BE0, physical address D217EBE0

a) Create a similar chart for a CPU data read of the word at virtual address 124A5DF4, assuming the page translation is in the L2 TLB, but not the L1 TLB, and the word is in memory, but not found in any cache.
b) Create a similar chart for a CPU data read of the word at virtual address 124A5DF4, still assuming the page translation is in the L2 TLB but not the L1 TLB, and the word is in memory but not found in any cache, but this time also assuming you converted the L2 cache to use the virtual address for its index and tag instead of the physical address. Would you make this change?

Question 2: (30 points)

Consider a hard disk drive has 10 platters where each platter has 2 surfaces. There are 50,000 tracks in each surface, and each track has 1,000 sectors on average. The size of each sector is 2,048 bytes. The rotational rate of this disk is 7,200 RPM, while the average seek time is 10 ms. The disk can approximately read 64 MB data from sectors in one second. Assume the controller overhead is 0.1 ms, and there is no queuing delay for this disk.

a) What is the capacity of this disk?
b) What is the average access time of this disk?