## CMSC611: Advanced Computer Architecture Extra Credit Homework 3

All parts of this assignment will use the following data, taken from a (real) run of valgrind on an application. The numbers given are inclusive (including all calls of the function, and any function that it calls). Assume two levels of cache, an L1 hit time of 1 cycle, L2 hit time of 40 cycles, memory access time of 200 cycles, and a branch penalty of 10 cycles. Changes mentioned in any question apply for that question only, and should not be carried forward to later questions.

## main():

Event	Short Name	Count
Calls	C <sub>m</sub>	1
Instruction Fetch	Ir <sub>m</sub>	7,371,916,291
Data Read Access	Dr <sub>m</sub>	2,132,375,654
Data Write Access	Dw <sub>m</sub>	692,582,065
L1 Instruction Fetch Misses	I1mr <sub>m</sub>	2,843
L1 Data Read Misses	D1mr <sub>m</sub>	2,017
L1 Data Write Misses	D1mw <sub>m</sub>	13,023
L1 Miss Sum	L1m <sub>m</sub>	17,883
L2 Instruction Read Misses	ILmr <sub>m</sub>	719
L2 Data Read Misses	DLmr <sub>m</sub>	322
L2 Data Write Misses	DLmw <sub>m</sub>	12,617
L2 Miss Sum	LLm <sub>m</sub>	13,657
Conditional Branches	Bc <sub>m</sub>	321,742,305
Mispredicted Cond. Branches	Bcm <sub>m</sub>	3,407,404
Indirect Branches	Bi <sub>m</sub>	98,326,304
Mispredicted Ind. Branches	Bim <sub>m</sub>	2,541,727
Total Mispredicted Branches	Bm <sub>m</sub>	5,949,131

## Sphere::intersect()

Event	Short Name	Count
Calls	Cs	9,555,396
Instruction Fetch	Ir <sub>s</sub>	5,744,882,374
Data Read Access	Dr <sub>s</sub>	1,530,528,738
Data Write Access	Dws	477,776,980
L1 Instruction Fetch Misses	I1mr <sub>s</sub>	6
L1 Data Read Misses	D1mr <sub>s</sub>	1
L1 Data Write Misses	D1mw <sub>s</sub>	0
L1 Miss Sum	L1m <sub>s</sub>	7
L2 Instruction Read Misses	ILmr <sub>s</sub>	6
L2 Data Read Misses	DLmr <sub>s</sub>	0
L2 Data Write Misses	DLmw <sub>s</sub>	0
L2 Miss Sum	LLm <sub>s</sub>	6
Conditional Branches	Bc <sub>s</sub>	97,279,766
Mispredicted Cond. Branches	Bcm <sub>s</sub>	925,966
Indirect Branches	Bis	0
Mispredicted Ind. Branches	Bim <sub>s</sub>	0
Total Mispredicted Branches	Bm <sub>s</sub>	925,966

- a) What is the overall branch misprediction rate?
- b) What is the misprediction rate within the Sphere::intersect() function?
- c) What is the overall L1 miss rate? The overall L2 miss rate?
- d) What is the average memory access time (AMAT) in cycles?
- e) What is the expected total number of cycles for this program?
- f) What is the expected total number of cycles spent in the Sphere::intersect() function?
- g) If the clock rate is 2 GHz, what is the total execution time of the program?
- h) If we could reduce the total execution time by a billion cycles, what would the overall speedup be?
- i) If we could make Sphere::intersect() 1.5x faster what would the overall speedup be?
- j) What would the expected overall speedup be if we could cut the L2 hit time to 10 cycles?
- k) What would the expected overall speedup be if we could cut the memory access time to 75 cycles?
- 1) What would the expected overall speedup be if we could cut the branch miss rate in half?
- m) The indirect branches are primarily due to virtual function calls. What would the expected overall speedup be if we could refactor the code to eliminate them without increasing the other cycle counts?
- n) What would the total execution time be without cache or branch prediction?

Suppose we introduce a new conditional load instruction that can replace a branch followed by a load with a single new instruction. The new instruction does not branch, so cannot be mispredicted, however, it will access its data memory argument even if it doesn't use it, so may increase the data access rate.

- o) If **all** of the conditional branches in Sphere::intersect() could use this new instruction, what speedup would you expect in the Sphere::intersect() function? Be sure to account for any changes in instruction count, data access count, and branch count.
- p) If you only use this new instruction in Sphere::intersect(), what is your expected total speedup?
- q) What is the expected total execution time with the new instruction?