Advanced Computer Architecture CMSC 611
Extra Credit HW2

Due at 1.05pm, Dec 3rd, 2012

(If you wish to **go green,** then you can submit the entire Homework electronically. Make sure you include the string "CMSC 611 Homework" in your subject line. Deadline remains the same) Please **DO NOT** email your homework to Dr. Olano!! **DO NOT** include him in the CC either!! There is a strong chance it won't be graded if you do!! **Send it only to <abhay1@umbc.edu>**

1) (30 points)
    a) What is seek time in a fixed disk? What is rotational latency?
    b) How does RAID increase data *availability* in a disk IO system? How does RAID increase data *reliability* in a disk IO system?
    c) What is a Vector operation? Give an example
    d) What is the primary advantage of adding a translation lookaside buffer (TLB)?
    e) What is the difference between a conflict miss and a compulsory miss for caches? How would you reduce each type?
    f) Define
        i. Out-of-order execution
        ii. Very long instruction word (VLIW)

2) (30 points)
    Assume you have a processor with an ideal CPI without memory stalls for each instruction type as follows: ALU=1, Load/Store=1.5, Branch=1.5, Jump=1. Consider an application which has an instruction mix of 30% ALU and logical operations, 40% load and store, 20% branch and 10% jump instructions.
    (a) Assume a 4-way set associative 1-level separate data and instruction cache with a miss rate of 20% (0.20) for data accesses and miss rate of 10% (0.10) for instructions, and a miss penalty of 40 cycles for both instruction and data caches (and assume a cache hit takes 1 cycle). What is the effective CPU time (or effective CPI with memory stalls) and the average memory access time for this application with this Cache organization?
    (b) Now consider a 2 level 4-way unified cache with a level l (L1) miss rate of 25% (0.25) and a level 2 (L2) local miss rate of 30% (0.30). Assume hit time in L1 is 1 cycle, assume miss penalty is 15 cycles if you miss in L1 and hit in L2 (i.e., hit time in L2 is 10 cycles), and assume miss penalty is 50 cycles if you miss in L2 (i.e., miss penalty in L2 is 50 cycles). Derive the equation for the effective CPU time (or effective CPI) and the average memory access time for the same instruction mix as part (a) for this cache organization.

    Which of the two designs (between part a and part b) gives a better performance? Explain your answer.

3) (40 points)

Consider a system with the following processor components and policies:

- A direct-mapped L1 data cache of size 4KB and block size of 16 bytes, indexed and tagged using physical addresses, and using a write-allocate, write-back policy
- A fully-associative data TLB with 4 entries and an LRU replacement policy
- Physical addresses of 32 bits, and virtual addresses of 40 bits
- Byte addressable memory
- Page size of 1MB

Part A

Which bits of the virtual address are used to obtain a virtual to physical translation from the TLB? Explain exactly how these bits are used to make the translation, assuming there is a TLB hit.

Part B

Which bits of the virtual or physical address are used as the tag, index, and block offset bits for accessing the L1 data cache? Explicitly specify which of these bits can be used directly from the virtual address without any translation.

Part C

The following lists part of the page table entries corresponding to a few virtual addresses (using hexadecimal notation). Protection bits of 01 imply read-only access and 11 implies read/write access. Dirty bit of 0 implies the page is not dirty. Assume the valid bits of all the following entries are set to 1.

Virtual page number		Physical page number	Protection bits	Dirty bits
1	FFFFF	CFC	11	0
2	FFFFE	CAC	11	0
3	FFFFD	CFC	11	0
4	FFFFC	CBA	11	0
5	FFFFB	CAA	11	0
6	FFFFA	CCA	01	0

The following table lists a stream of eight data loads and stores to virtual addresses by the processor (all addresses are in hexadecimal). Complete the rest of the entries in the table corresponding to these loads and stores using the above information and your solutions to parts A and B. For the data TLB hit, data cache hit, and protection violation columns, specify "yes" or "no." Assume initially the data TLB and data cache are both empty.

	Processor load/store to virtual address	Corresponding physical address	Part of the physical address used to index the data cache	Data TLB hit?	Data cache hit?	Protection violation?	Dirty bit
1	Store FFFFF ABAC1						
2	Store FFFFC ECAB1						
3	Load FFFFF BAAE3						
4	Load FFFFB CEBC3						
5	Store FFFFE AAFA1						
6	Store FFFFC AABC9						
7	Load FFFFD BAAE2						
8	Store FFFFA ABAC4						