CMSC 611

Introduction / Evaluating Cost

Levels of Behavior Representation

High Level Language Program

Compiler

Assembly Language Program

Assembler

Machine Language Program

Machine Interpretation

Control Signal Specification

temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;

```
lw   $15, 0($2)
lw   $16, 4($2)
sw   $16, 0($2)
sw   $15, 4($2)
```

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

ALUOP[0:3] <= InstReg[9:11] & MASK

Slide: David Patterson, UCB

Levels of Abstraction

- S/W and H/W consists of hierarchical layers of abstraction, each hides details of lower layers from the above layer
- The instruction set arch. abstracts the H/W and S/W interface and allows many implementation of varying cost and performance to run the same S/W

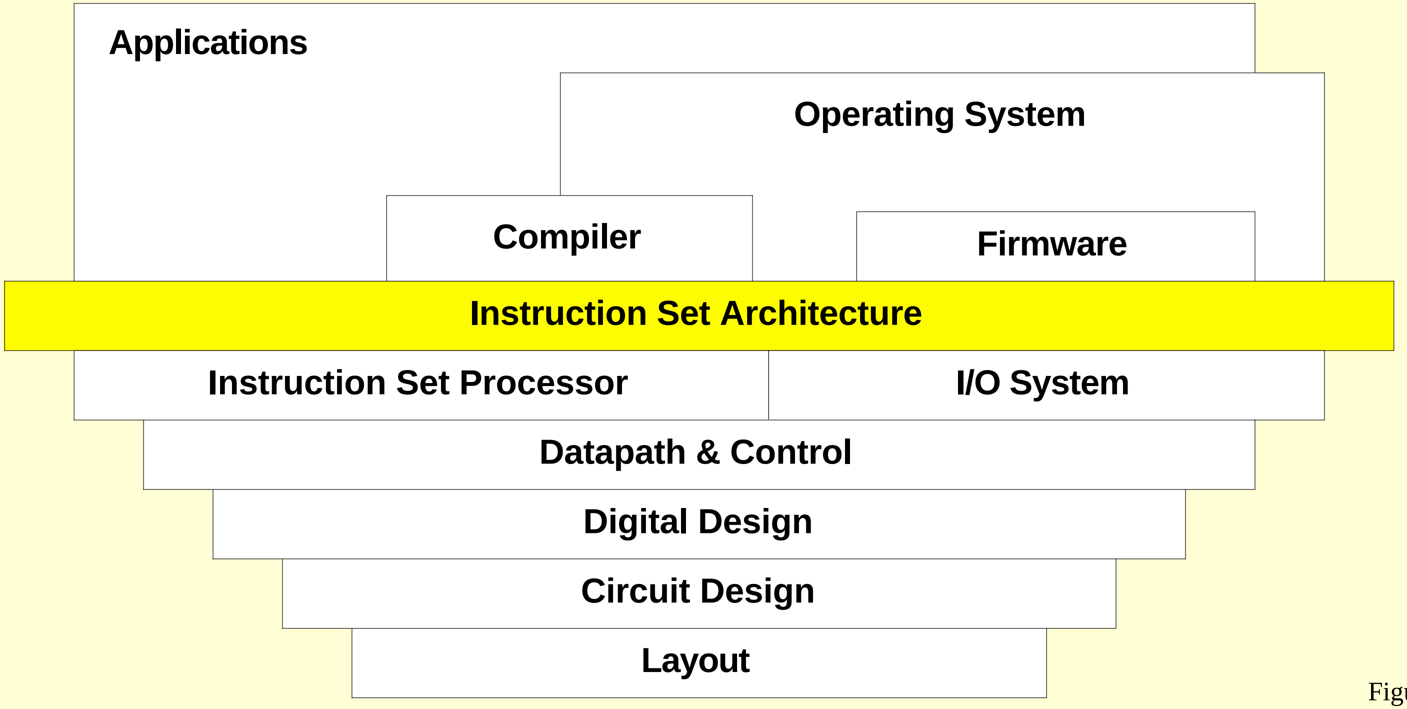


Figure: David Patterson, UCB

Forces on Computer Architecture

- Programming languages might encourage architecture features to improve performance and code size, e.g. Fortran and Java
- Operating systems rely on the hardware to support essential features such as semaphores and memory management
- Technology always raises the bar for what could be done and changes design's focus
- Applications usually derive capabilities and constrains
- History provides the starting point, filters out mistakes

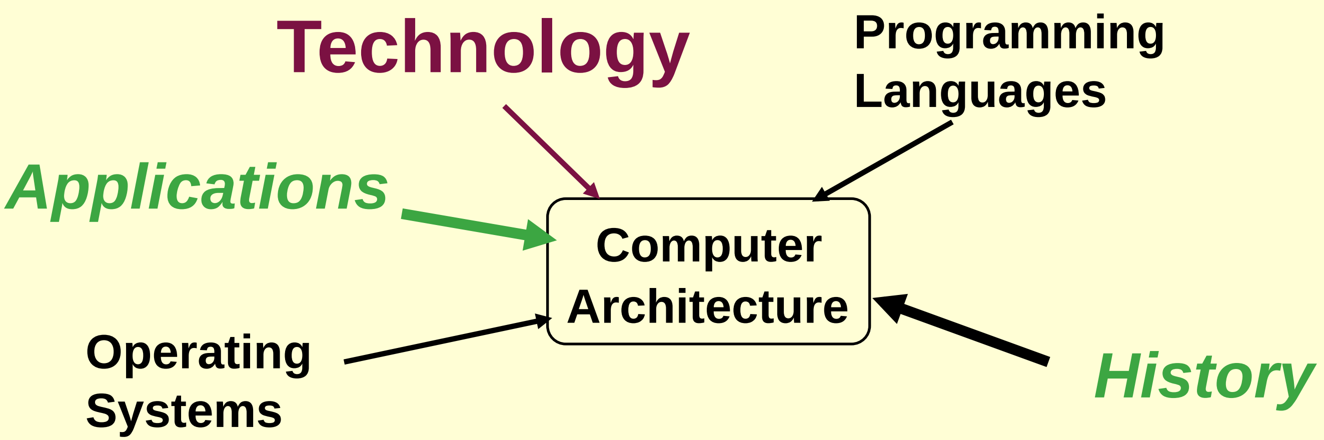


Figure: David Patterson, UCB

Technology – dramatic change

- Processor
  - logic capacity: about 30% increase per year
  - clock rate: about 20% increase per year

Higher logic density gave room for instruction pipeline & cache

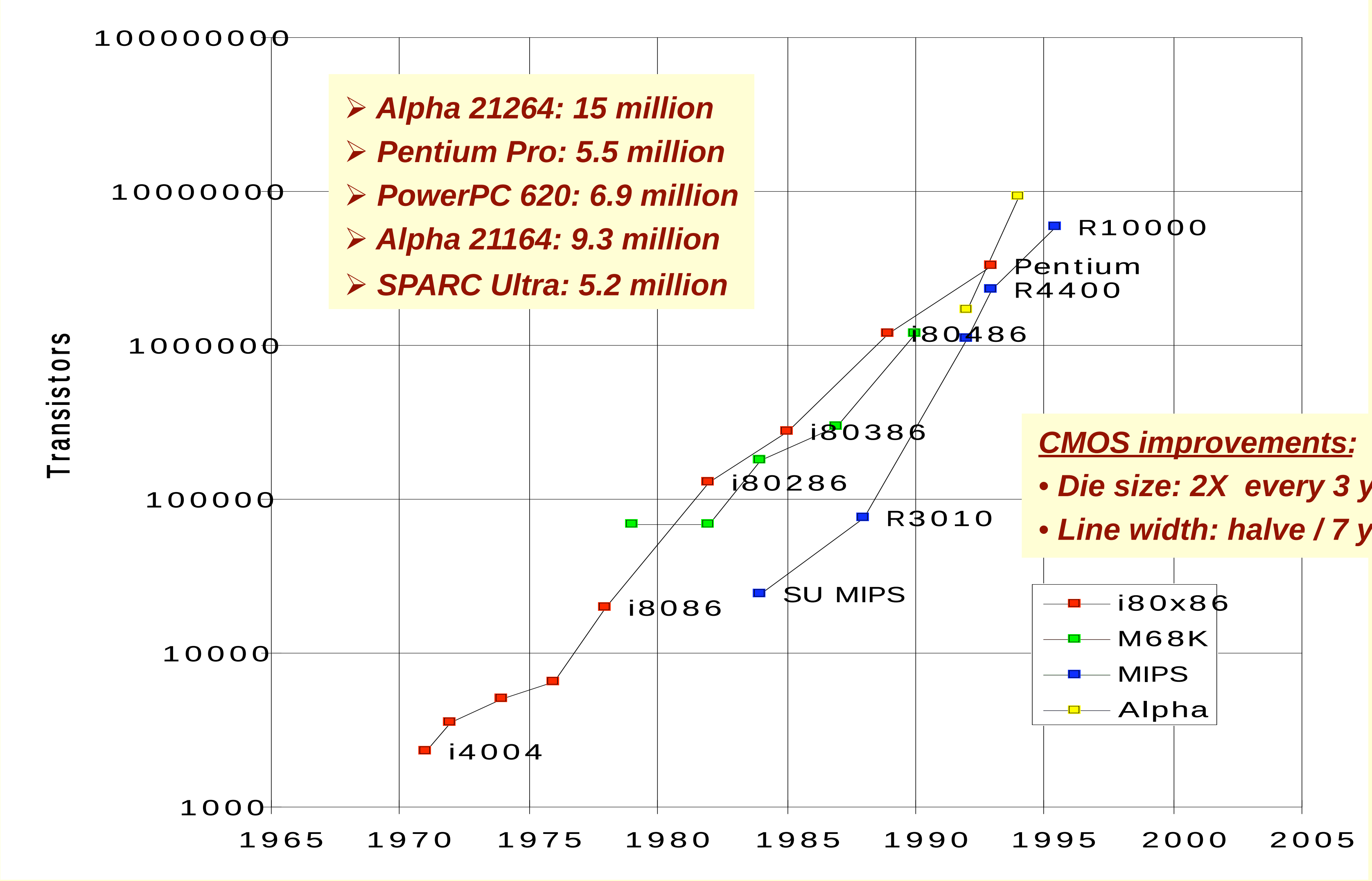
- Memory
  - DRAM capacity: about 60% increase per year (4x / 3 years)
  - Memory speed: about 10% increase per year
  - Cost per bit: about 25% improvement per year

Performance optimization no longer implies smaller programs

- Disk
  - Capacity: about 60% increase per year

Computers became lighter and more power efficient

Technology Impact



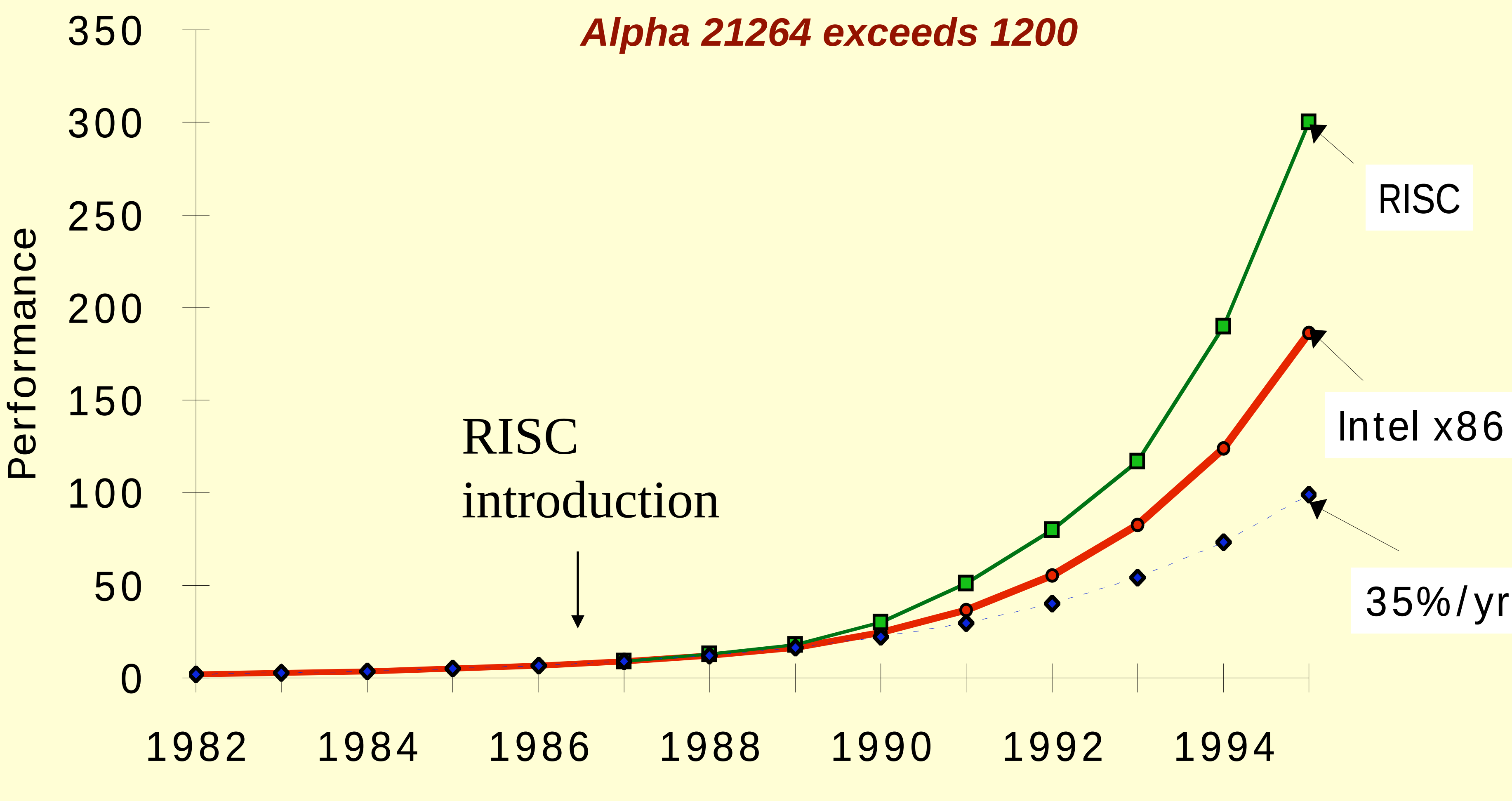
- Alpha 21264: 15 million
- Pentium Pro: 5.5 million
- PowerPC 620: 6.9 million
- Alpha 21164: 9.3 million
- SPARC Ultra: 5.2 million

CMOS improvements:

- *Die size: 2X every 3 yrs*
- *Line width: halve / 7 yrs*

Figure: David Patterson, UCB

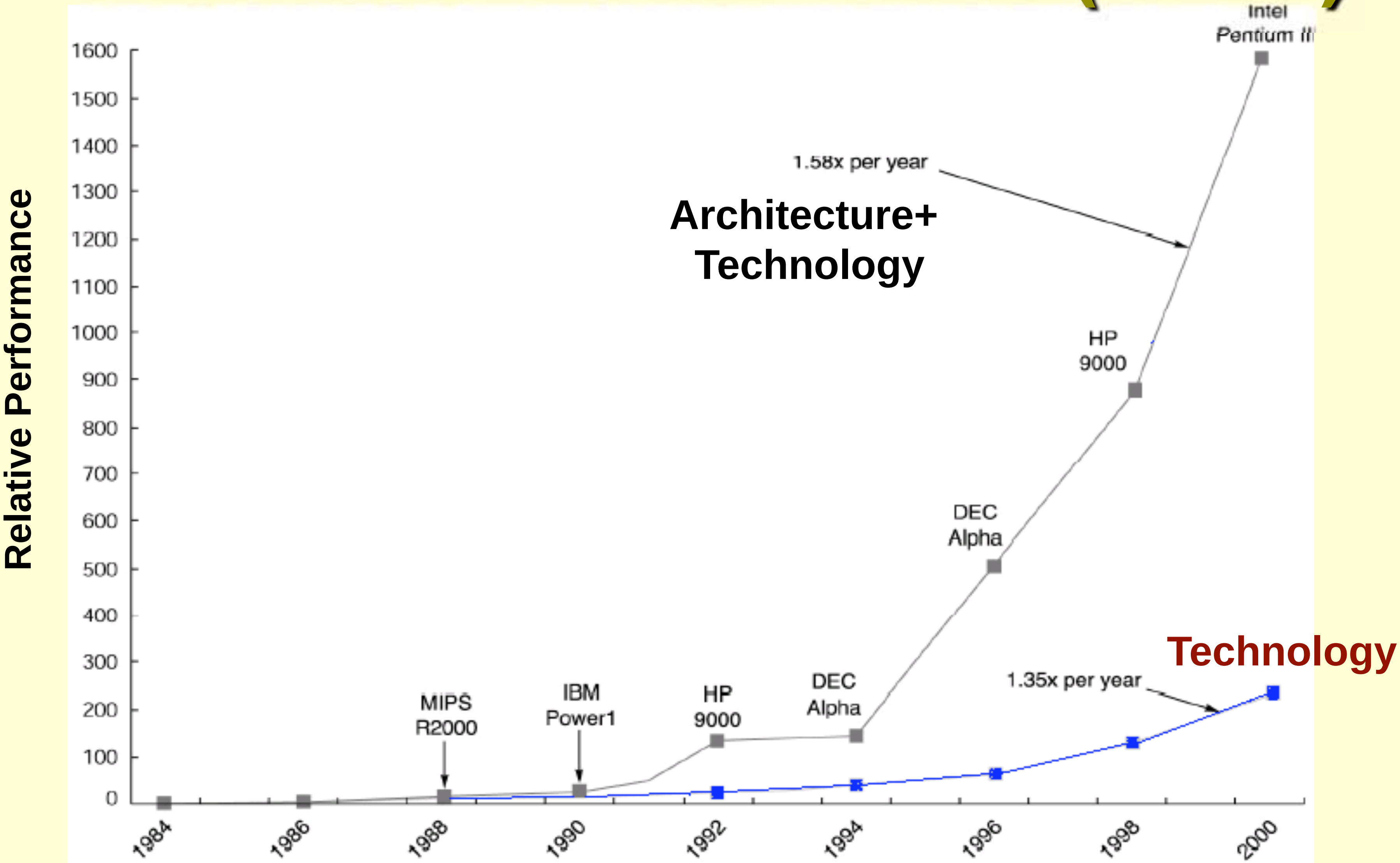
Processor Performance (SPEC)



Performance now improves ~ 50% per year (2x every 1.5 years)

Slide: David Patterson, UCB

Processor Performance (SPEC)



Relying on technology alone would have kept us 8 years behind

One Architectural Factor

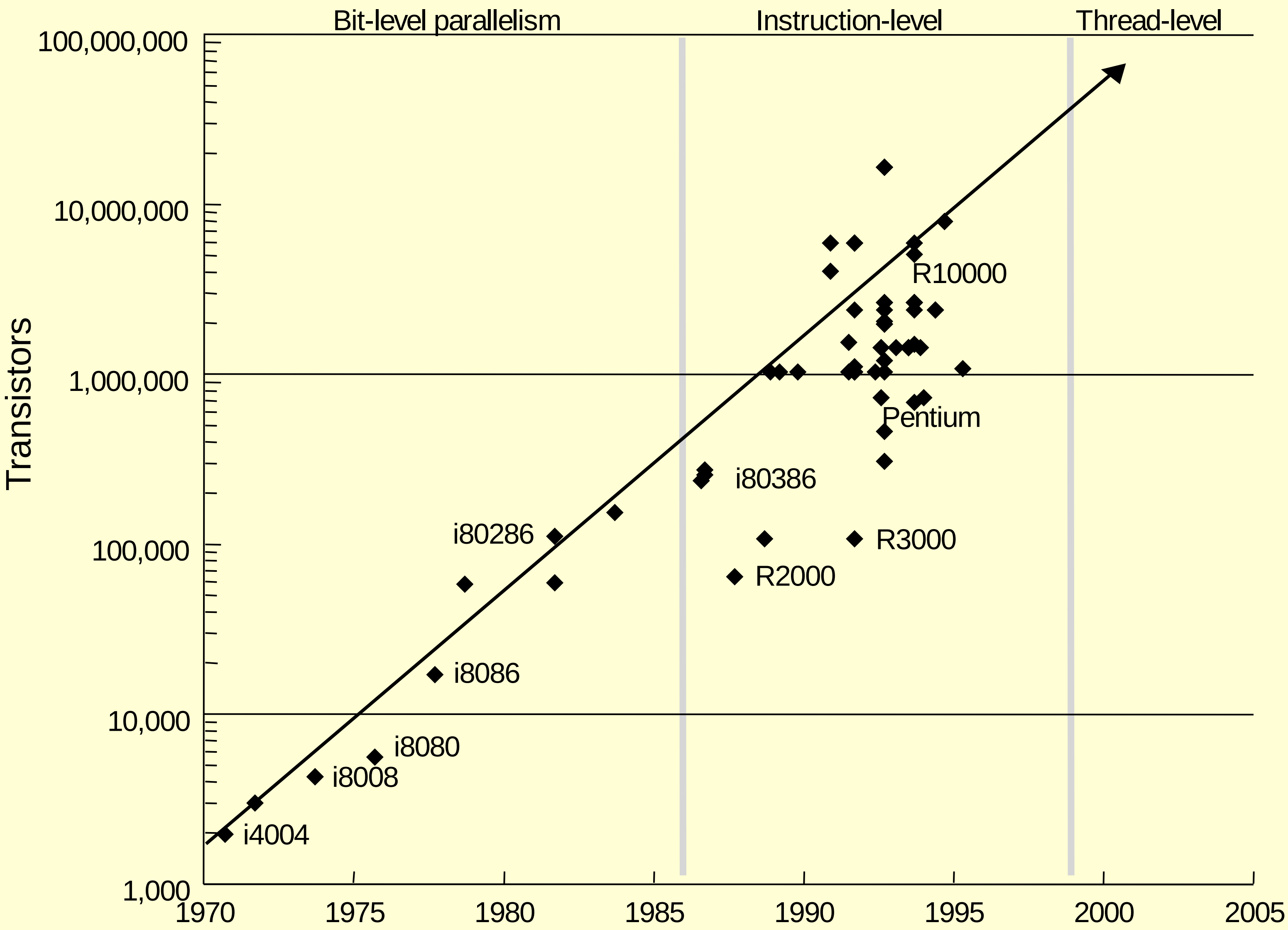
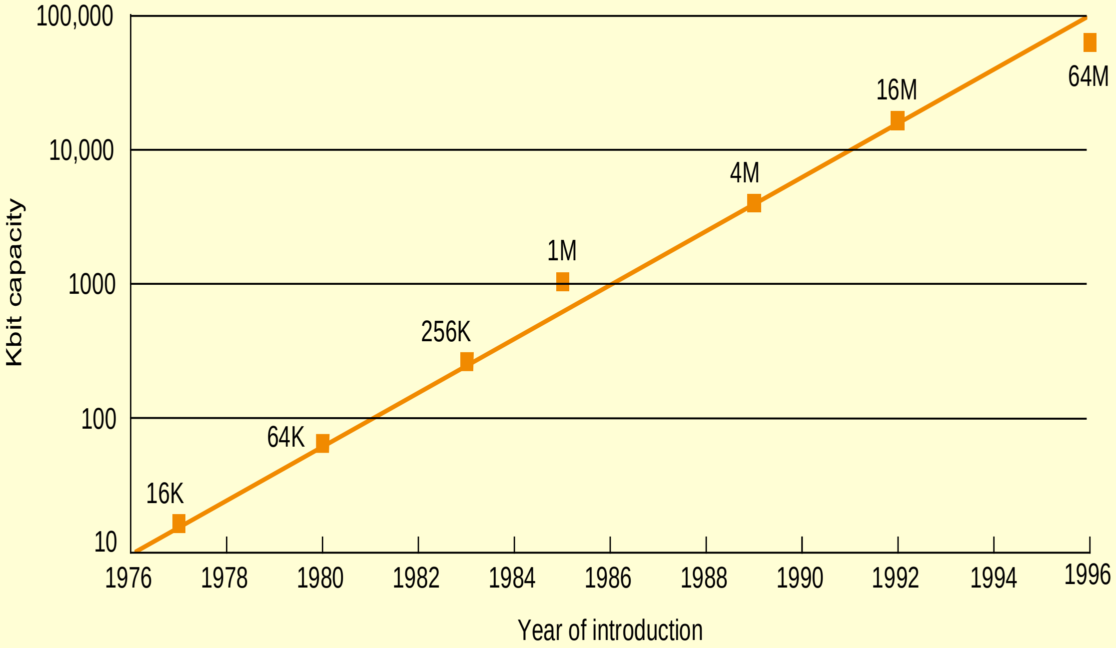


Figure: David Culler, UCB

Technology Impact on Design

- DRAM capacity 4x / 3 yrs; 16,000x in 20 yrs!
- Programming concern: cache not RAM size
- Processor organization becoming main focus for performance optimization
- HW designer focus not only performance but functional integration and power consumption (e.g. system on a chip)



Year	Size	Cyc Time
1980	64 K	250 µs
1983	256 K	220 µs
1986	1 M	90 µs
1989	4 M	165 ns
1992	16 M	145 ns
1996	64 M	120 ns
2000	256 M	100 ns

Computer Engineering Methodology

Cost and performance are the main evaluation metrics for a design quality

Integrated Circuits: Fueling Innovation

- Chips begins with silicon, found in sand
- Silicon does not conduct electricity well and thus called semiconductor
- A special chemical process can transform tiny areas of silicon to either:
  - Excellent conductors of electricity (like copper)
  - Excellent insulator from electricity (like glass)
  - Areas that can conduct or insulate under a special condition (a switch)
- A transistor is simply an on/off switch controlled by electricity
- Integrated circuits combines dozens of hundreds of transistors in a chip

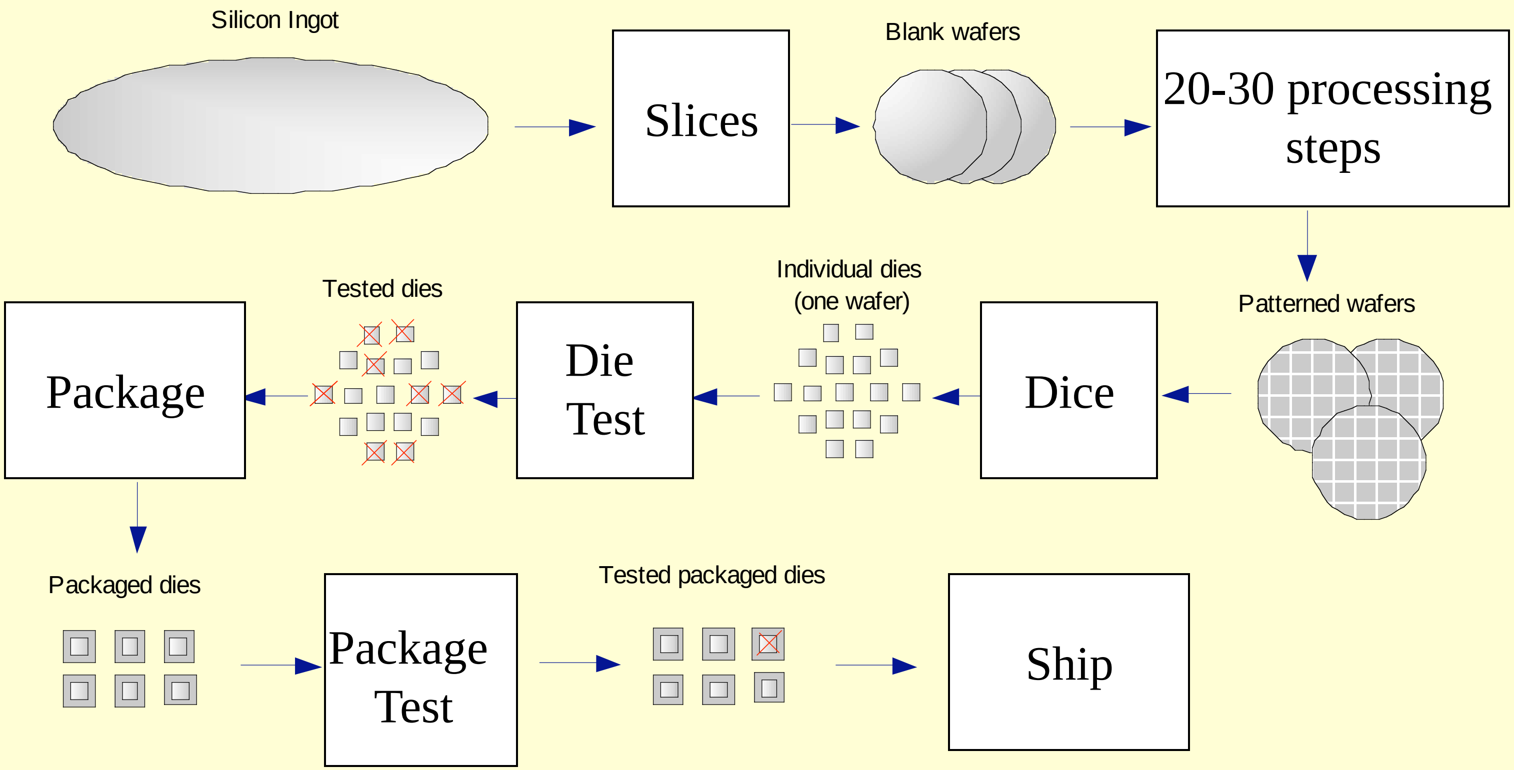
Integrated Circuits: Fueling Innovation

- Technology innovations over time

Year	Technology used in computers	Relative performance/unit cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuits	900
1995	Very large-scale integrated circuit	2,400,000

Advances of the IC technology affect H/W and S/W design philosophy

Microelectronics Process

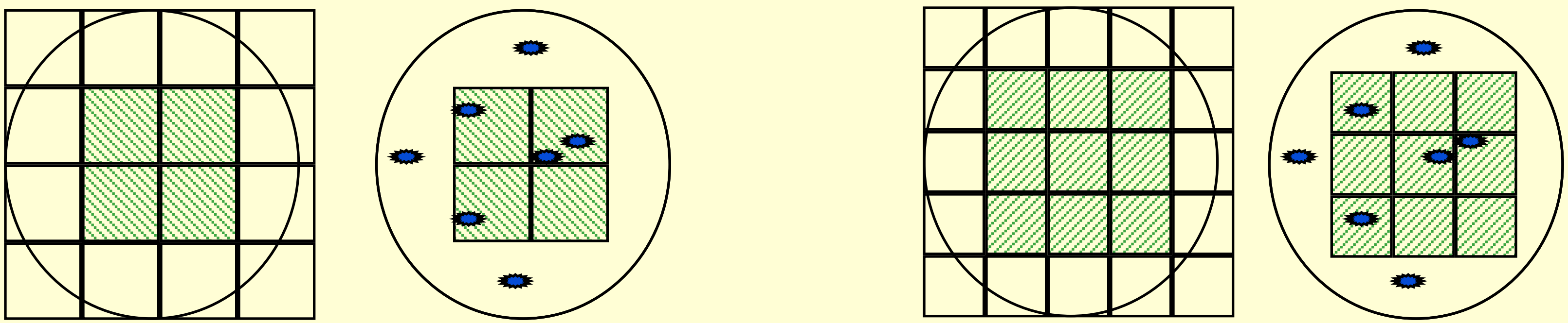


- Silicon ingots:
  - 6-12 inches in diameter and about 12-24 inches long
- Impurities in the wafer can lead to defective devices and reduces the yield

Integrated Circuits Costs

$$\text{Dies\_per\_Wafer} = \frac{\pi \times (\text{Wafer\_diameter}/2)^2}{\text{Die\_Area}} - \frac{\pi \times \text{Wafer\_Diameter}}{\sqrt{2 \times \text{Die\_Area}}}$$

$$\text{Die\_Yield} = \text{Wafer\_Yield} \times \left[1 + \frac{\text{Defects\_per\_Unit\_Area} * \text{Die\_Area}}{\alpha}\right]^{-\alpha}$$



$$\text{Die\_Cost} = \frac{\text{Wafer\_Cost}}{\text{Dies\_per\_Wafer} \times \text{Die\_Yield}}$$

Die cost roughly goes with die area^4

$$\text{IC\_Cost} = \frac{\text{Die\_Cost} + \text{Testing\_Cost} + \text{Packing\_Cost}}{\text{Final\_Test\_Yield}}$$