

CMSC 611

Introduction / Evaluating Cost

Some material adapted from Mohamed Younis, UMBC CMSC 611 Spr 2003 course slides

Some material adapted from David Culler, UC Berkeley CS252, Spr 2002 course slides, © 2002 UC Berkeley

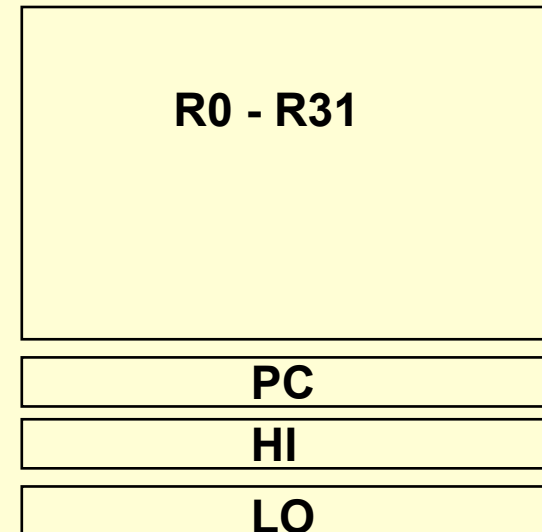
Some material adapted from Hennessy & Patterson / © 2003 Elsevier Science

MIPS R3000 ISA (Summary)

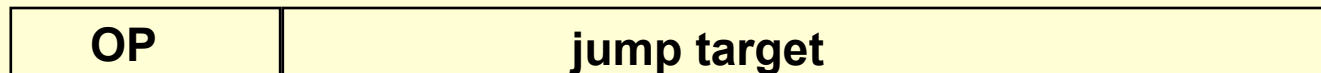
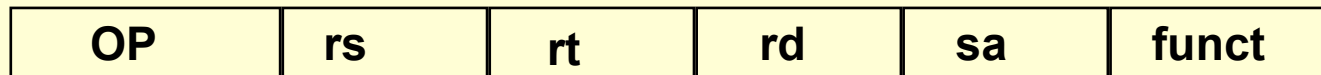
- Instruction Categories

- Load/Store
- Computational
- Jump and Branch
- Floating Point
 - coprocessor
- Memory Management
- Special

Registers



3 Instruction Formats: all 32 bits wide



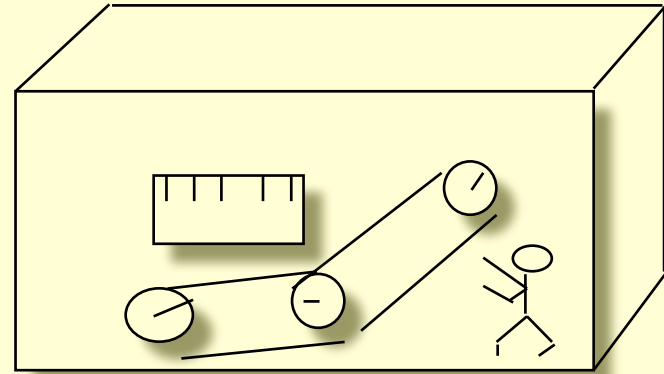
Machine Organization

- Capabilities & performance characteristics of principal functional units (e.g., Registers, ALU, Shifters, Logic Units, ...)
- Ways in which these components are interconnected
- Information flows between components
- Logic and means by which such information flow is controlled
- Choreography of functional units to realize the instruction set architecture
- Register Transfer Level Description

Logic Designer's View

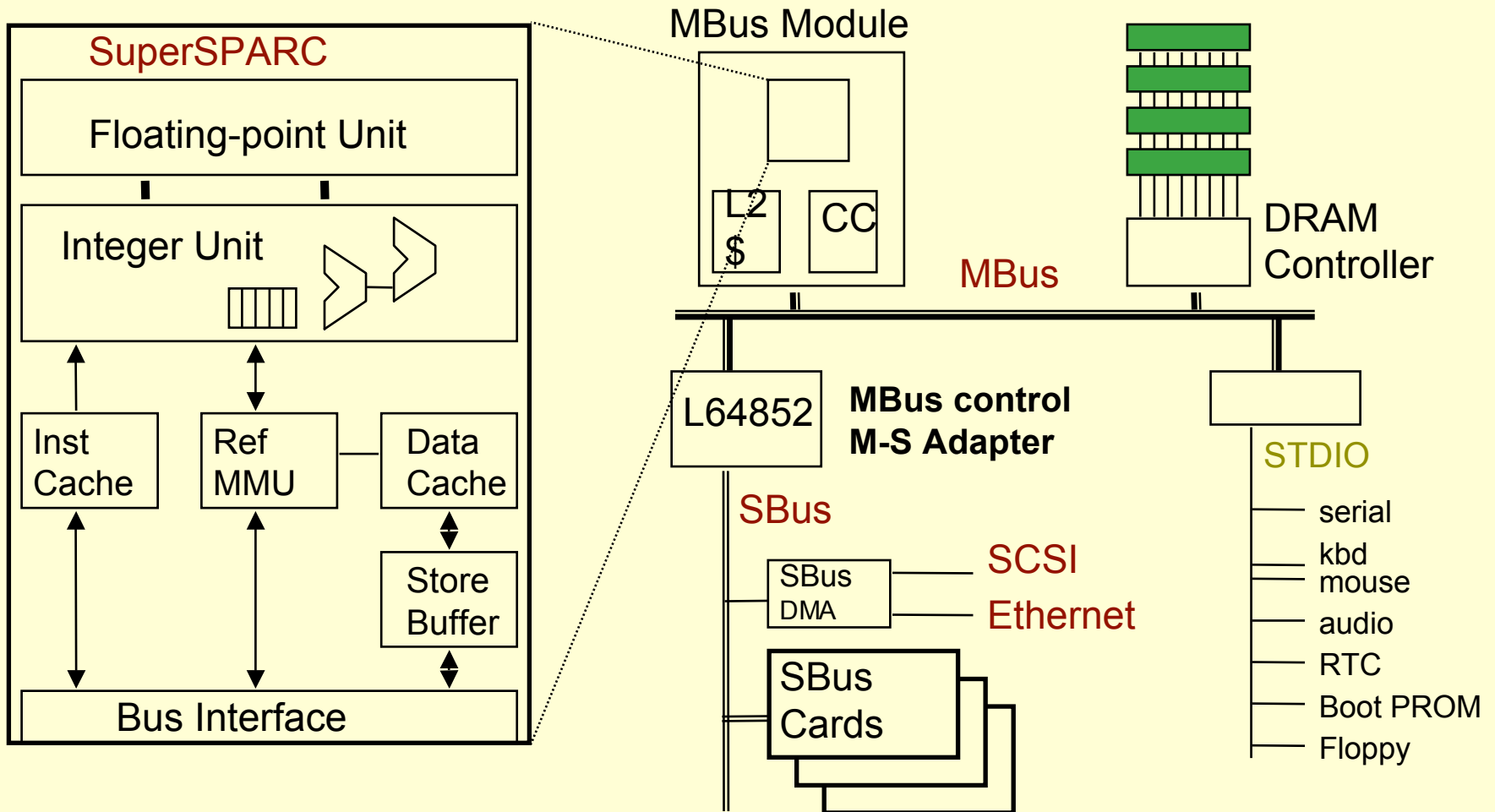
ISA Level

Functional Units & Interconnect

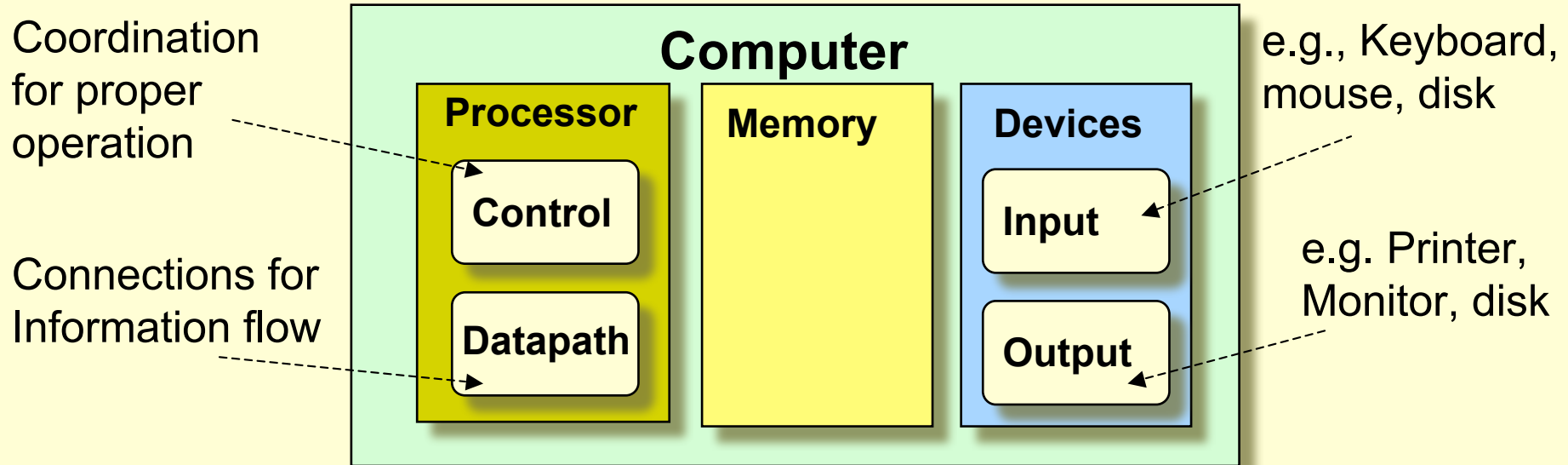


Example Organization

- TI SuperSPARCtm TMS390Z50 in Sun SPARCstation20



General Comp Organization



- Every piece of every computer, past and present: input, output, memory, datapath and control
- The design approach is constrained by the cost and size and capabilities required from every component
- An example design target can be 25% of cost on Processor, 25% of cost on minimum memory size, rest on I/O devices, power supplies, and chassis

Levels of Behavior Representation

High Level Language Program

Compiler

Assembly Language Program

Assembler

Machine Language Program

Machine Interpretation

Control Signal Specification

```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

lw \$15, 0(\$2)

lw \$16, 4(\$2)

sw \$16, 0(\$2)

sw \$15, 4(\$2)

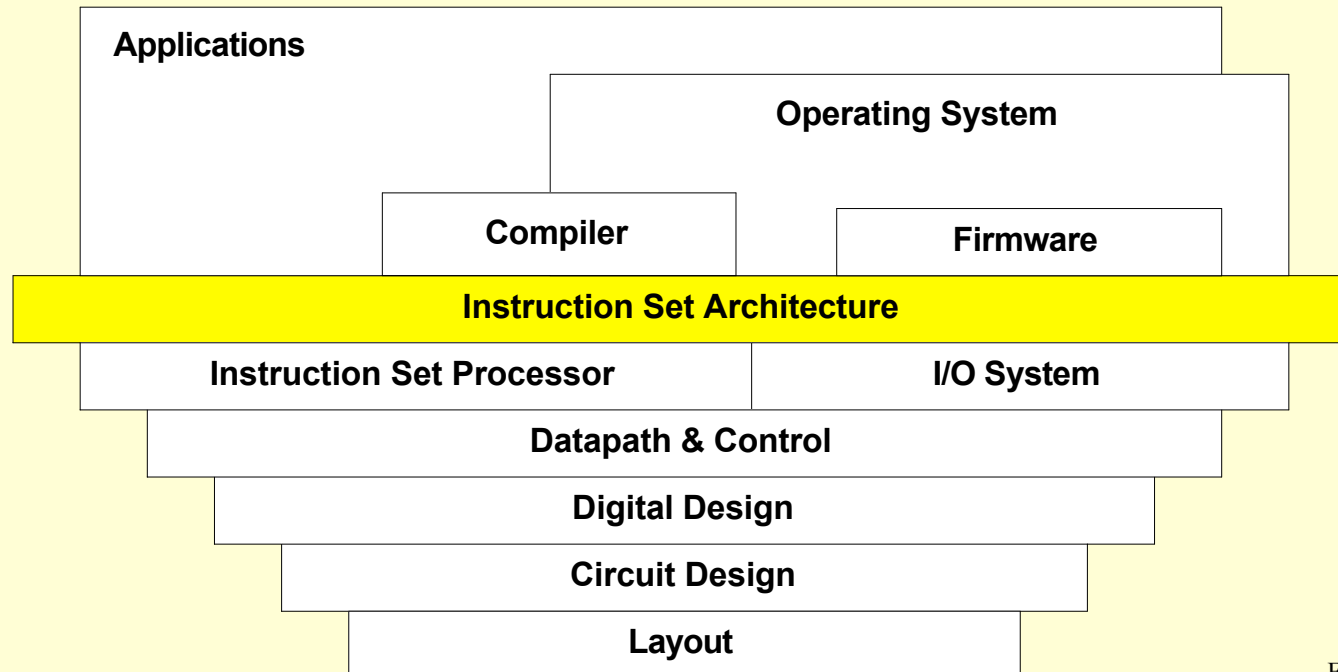
```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

ALUOP[0:3] <= InstReg[9:11] & MASK

- o
- o

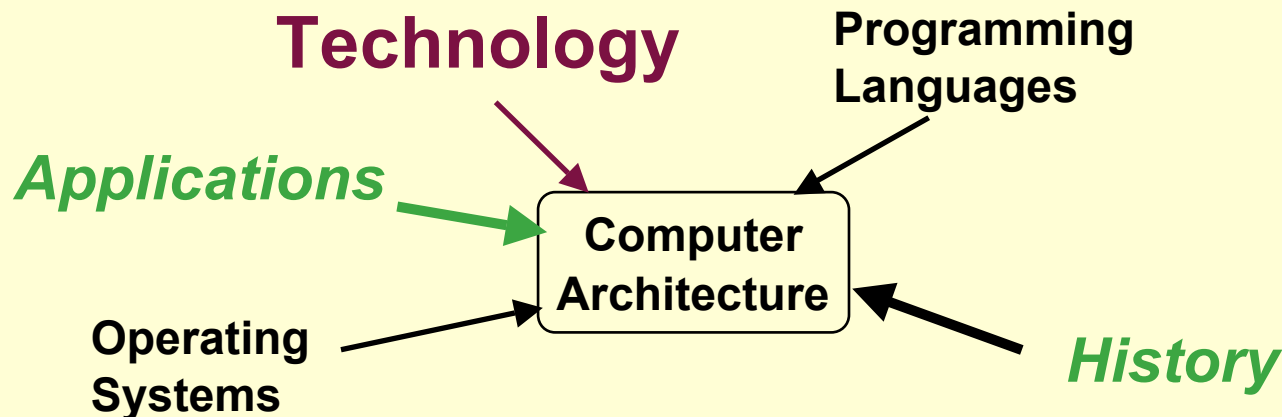
Levels of Abstraction

- S/W and H/W consists of hierarchical layers of abstraction, each hides details of lower layers from the above layer
- The instruction set arch. abstracts the H/W and S/W interface and allows many implementation of varying cost and performance to run the same S/W



Forces on Computer Architecture

- Programming languages might encourage architecture features to improve performance and code size, e.g. Fortran and Java
- Operating systems rely on the hardware to support essential features such as semaphores and memory management
- Technology always raises the bar for what could be done and changes design's focus
- Applications usually derive capabilities and constrains
- History provides the starting point, filters out mistakes



Technology – dramatic change

- Processor
 - logic capacity: about 30% increase per year
 - clock rate: about 20% increase per year

Higher logic density gave room for instruction pipeline & cache

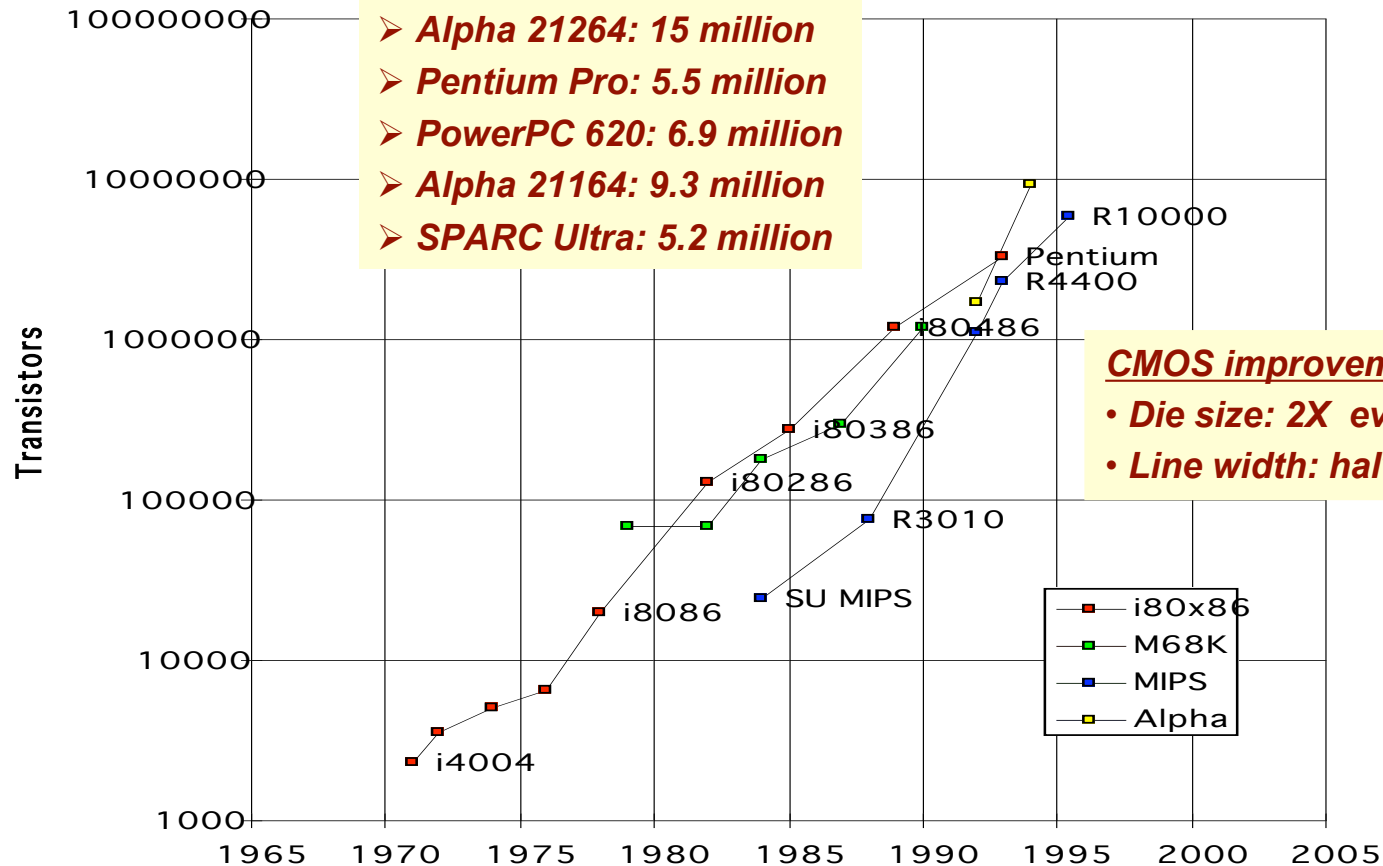
- Memory
 - DRAM capacity: about 60% increase per year
(4x / 3 years)
 - Memory speed: about 10% increase per year
 - Cost per bit: about 25% improvement per year

Performance optimization no longer implies smaller programs

- Disk
 - Capacity: about 60% increase per year

Computers became lighter and more power efficient

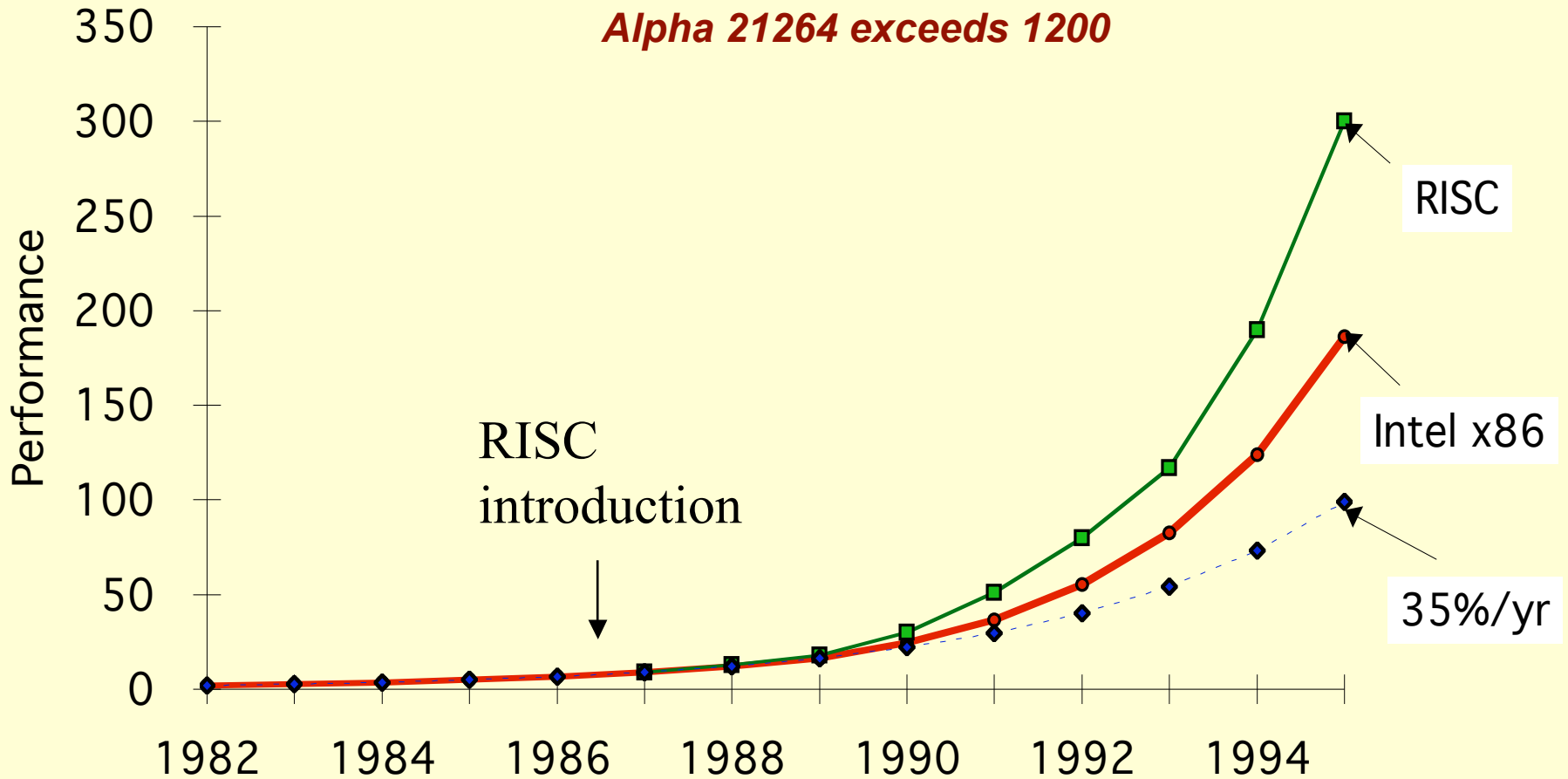
Technology Impact



In ~1985 the single-chip processor and the single-board computer emerged
 In the 2004+ timeframe, today's mainframes may be a single-chip computer

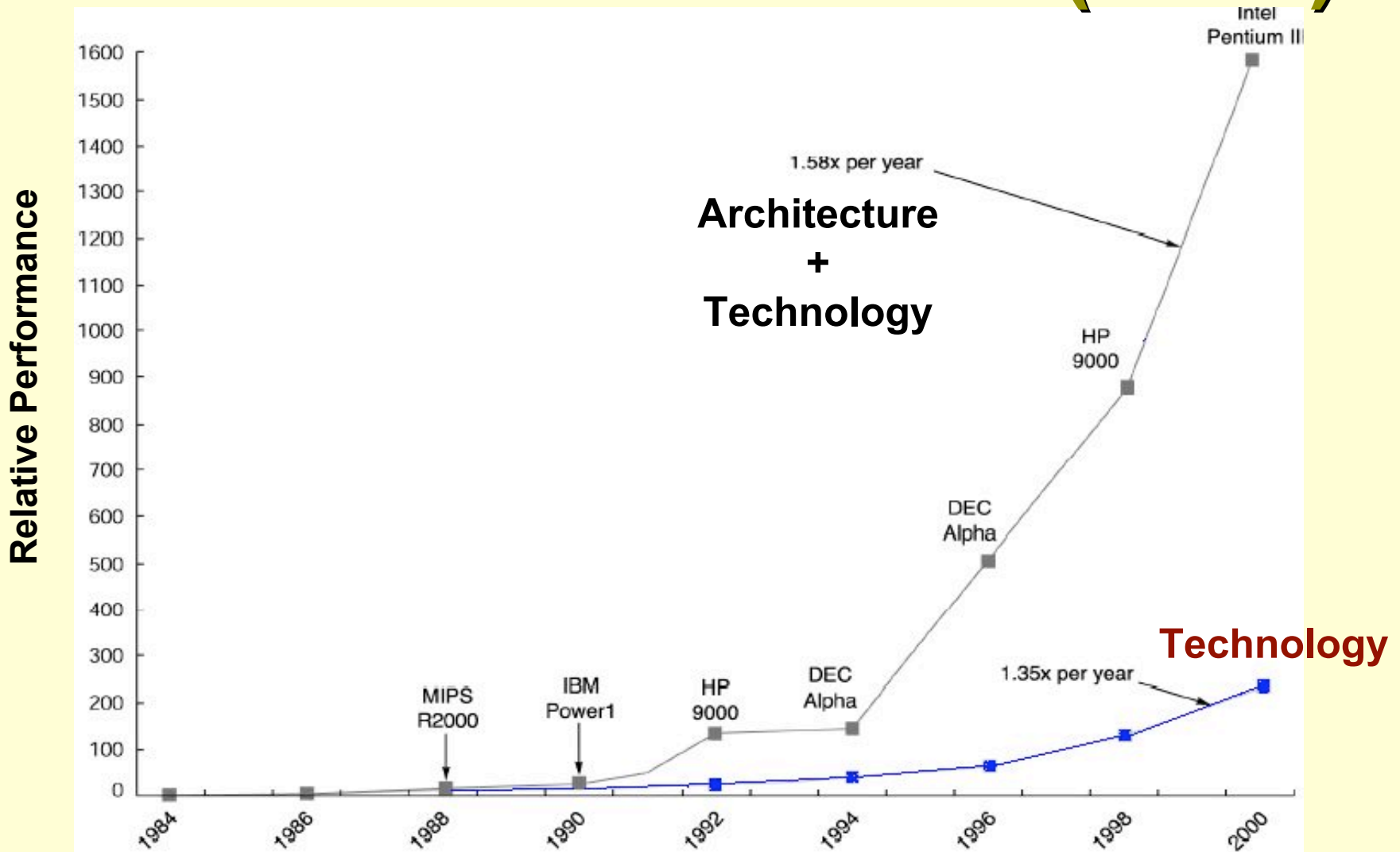
Processor Performance (SPEC)

Alpha 21264 exceeds 1200



Performance now improves ~ 50% per year (2x every 1.5 years)

Processor Performance (SPEC)



Relying on technology alone would have kept us 8 years behind

One Architectural Factor

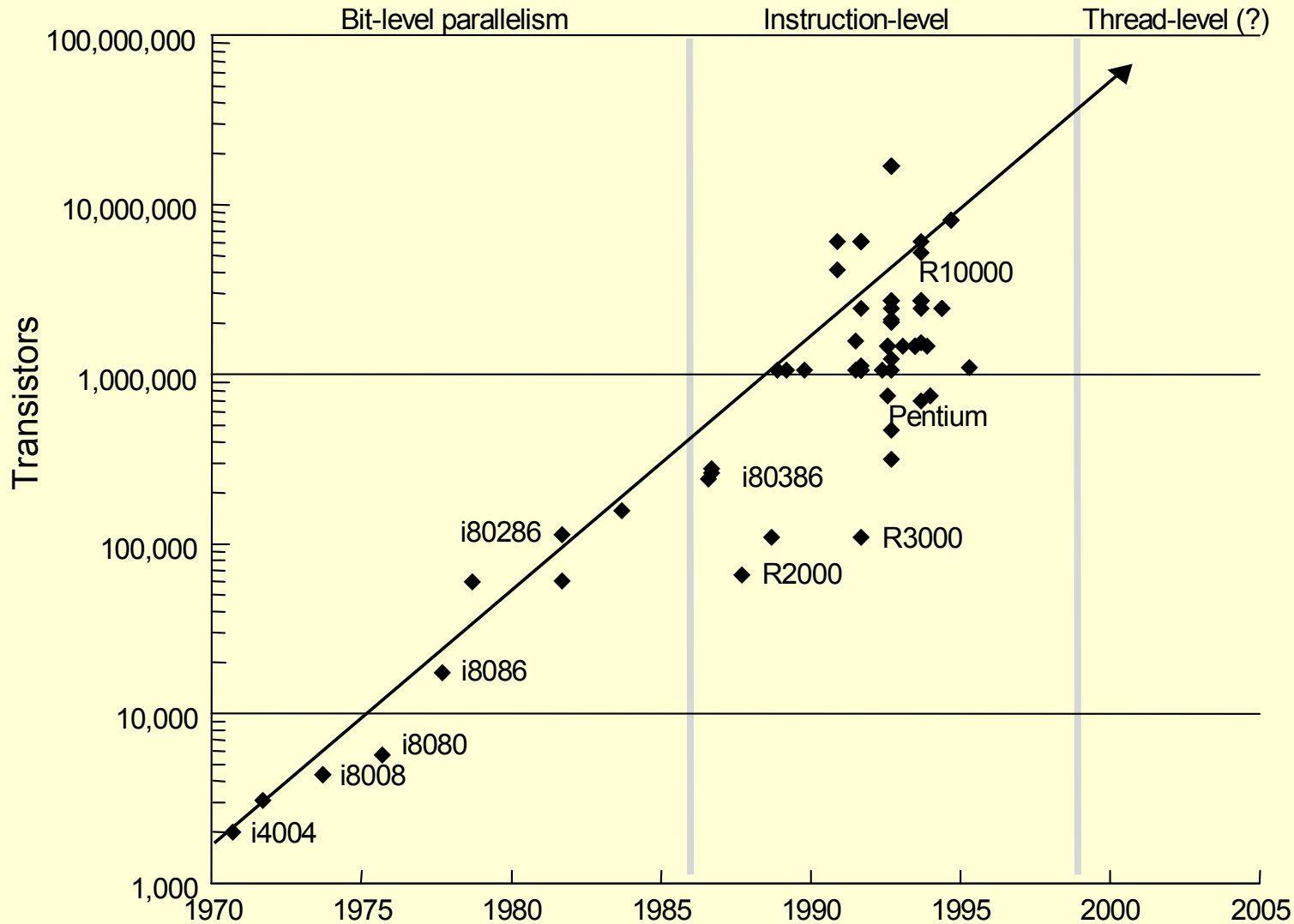
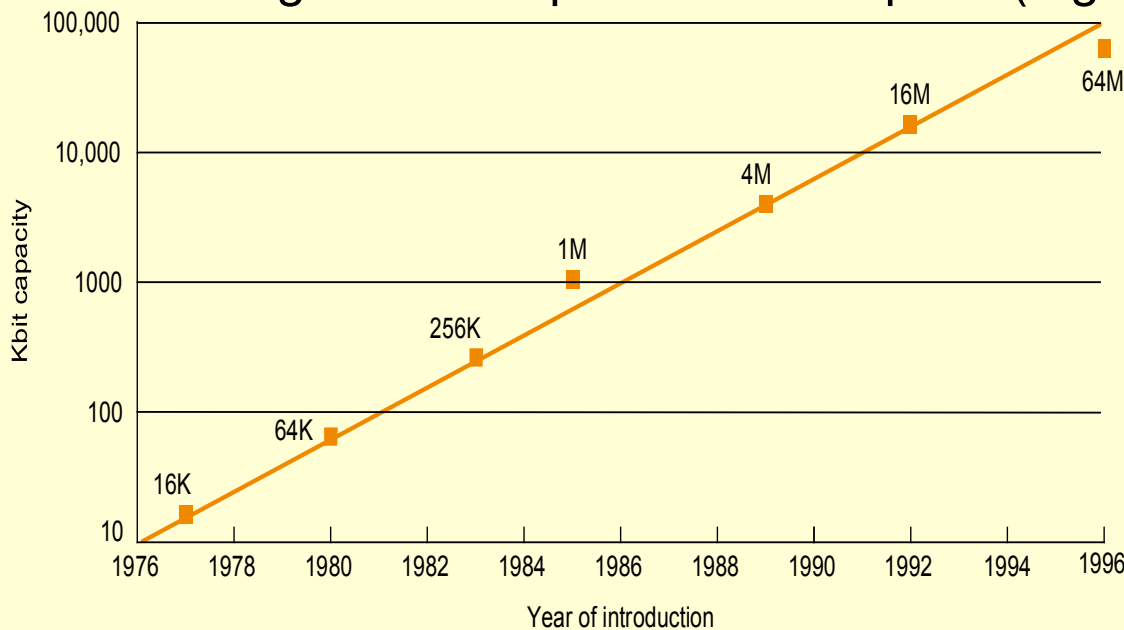


Figure: David Culler, UCB

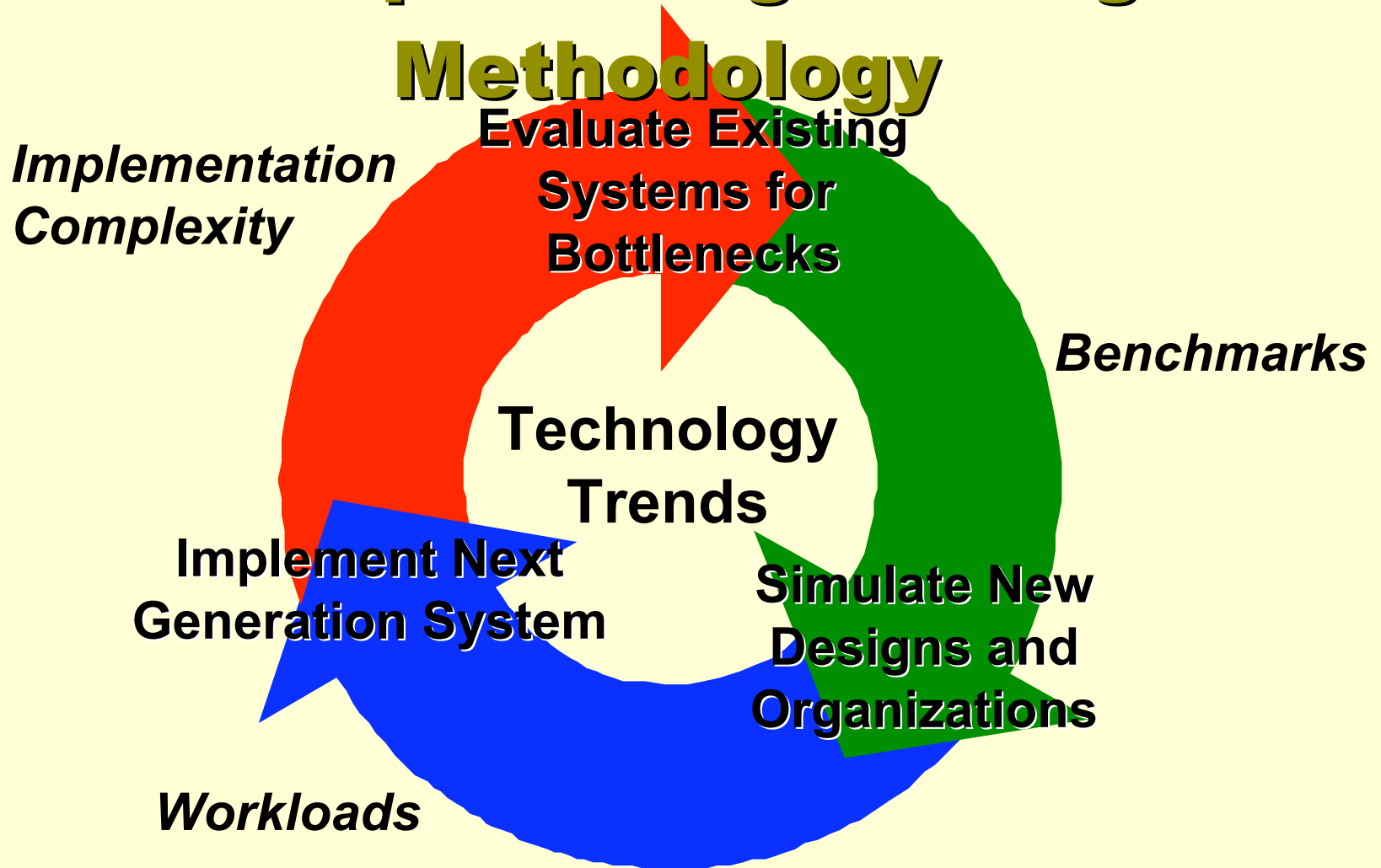
Technology Impact on Design

- DRAM capacity 4x / 3 yrs; 16,000x in 20 yrs!
- Programming concern: cache not RAM size
- Processor organization becoming main focus for performance optimization
- HW designer focus not only performance but functional integration and power consumption (e.g. system on a chip)



<u>Year</u>	<u>Size(Mb)</u>	<u>Cyc time</u>
1980	0.0625	250 ns
1983	0.25	220 ns
1986	1	190 ns
1989	4	165 ns
1992	16	145 ns
1996	64	120 ns
2000	256	100 ns

Computer Engineering



Cost and performance are the main evaluation metrics for a design quality

Integrated Circuits: Fueling

Innovation

- Chips begins with silicon, found in sand
- Silicon does not conduct electricity well and thus called semiconductor
- A special chemical process can transform tiny areas of silicon to either:
 - Excellent conductors of electricity (like copper)
 - Excellent insulator from electricity (like glass)
 - Areas that can conduct or insulate under a special condition (a switch)
- A transistor is simply an on/off switch controlled by electricity
- Integrated circuits combines dozens of hundreds of transistors in a chip

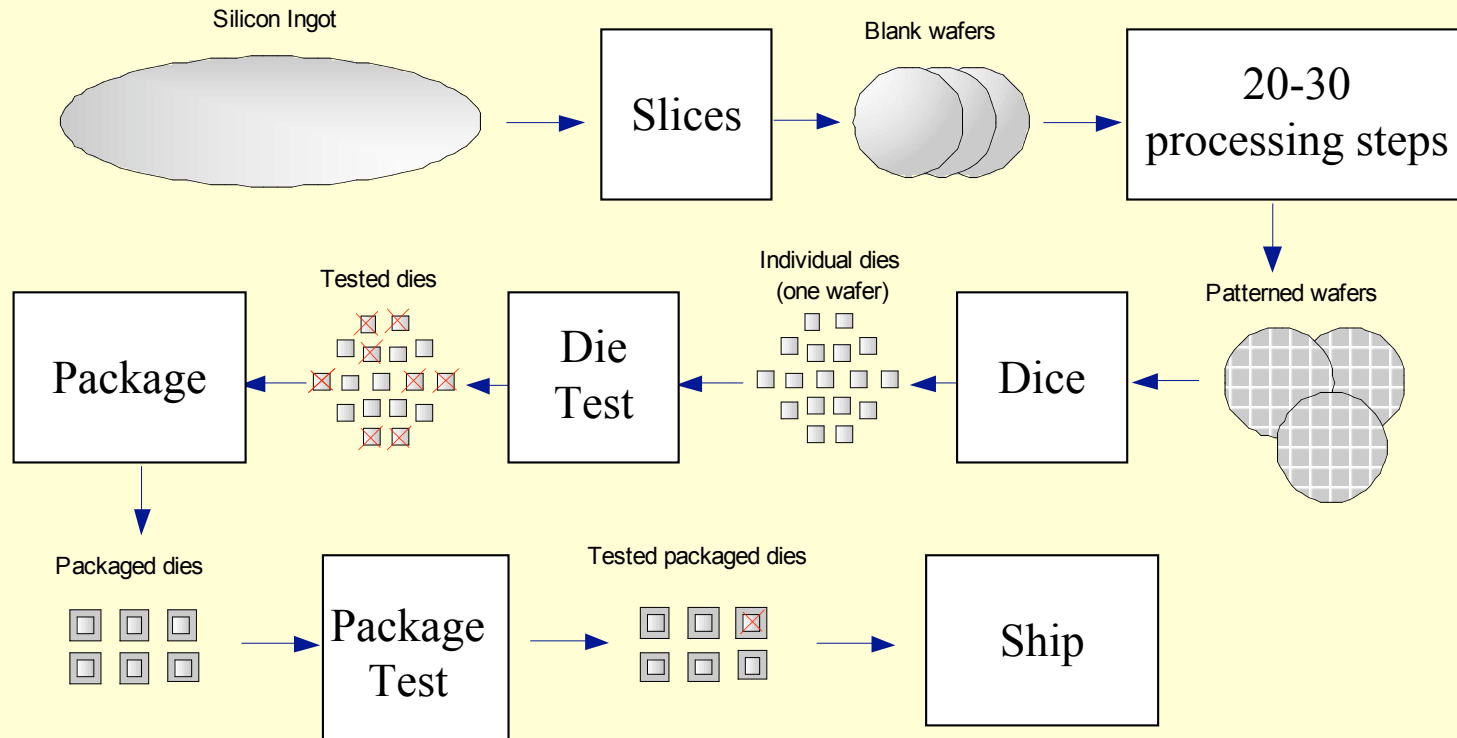
Integrated Circuits: Fueling Innovation

- Technology innovations over time

Year	Technology used in computers	Relative performance/unit cost
1951	Vacuum tube	1
1965	Transistor	35
1975	Integrated circuits	900
1995	Very large-scale integrated circuit	2,400,000

Advances of the IC technology affect H/W and S/W design philosophy

Microelectronics Process

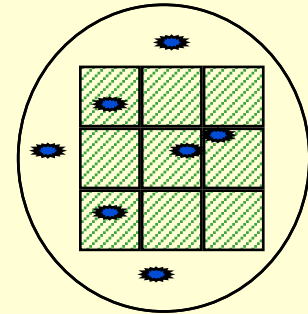
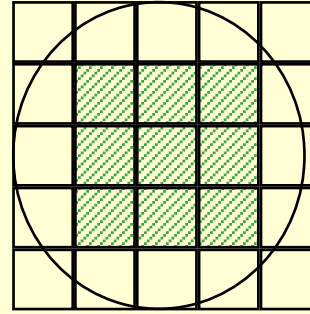
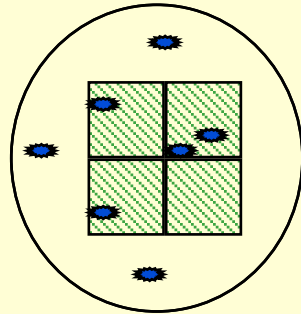
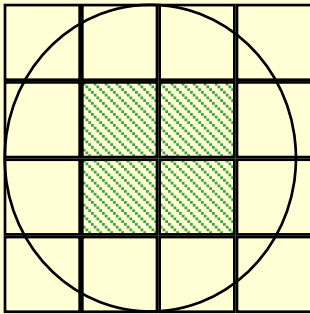


- Silicon ingots:
 - 6-12 inches in diameter and about 12-24 inches long
- Impurities in the wafer can lead to defective devices and reduces the yield

Integrated Circuits Costs

$$\text{Dies per Wafer} = \frac{\pi \times (\text{Wafer - diameter}/2)^2}{\text{Die Area}} - \frac{\pi \times \text{Wafer - diameter}}{\sqrt{2} \times \text{Die Area}}$$

$$\text{Die Yield} = \text{Wafer yield} \times \left[1 + \frac{\text{Defects_per_unit_area} * \text{Die_Area}}{\alpha} \right]^{-\alpha}$$



$$\text{Die Cost} = \frac{\text{Wafer Cost}}{\text{Dies per Wafer} \times \text{Die Yield}}$$

Die cost roughly goes with die area⁴

$$\text{IC Cost} = \frac{\text{Die Cost} + \text{Testing Cost} + \text{Packing Cost}}{\text{Final Test Yield}}$$

Real World Examples

Chip	Layers	Wafer cost	Defect/cm ²	Area (mm ²)	Dies/Wafer	Yield	Die Cost
386DX	2	\$900	1.0	43	360	71%	\$4
486DX2	3	\$1200	1.0	81	181	54%	\$12
PowerPC 601	4	\$1700	1.3	121	115	28%	\$53
HP PA 7100	3	\$1300	1.0	196	66	27%	\$73
DEC Alpha	3	\$1500	1.2	234	53	19%	\$149
SuperSPARC	3	\$1700	1.6	256	48	13%	\$272
Pentium	3	\$1500	1.5	296	40	9%	\$417

**From "Estimating IC Manufacturing Costs," by Linley Gwennap,
Microprocessor Report, August 2, 1993, p. 15**

Costs and Trends in Cost

- Understanding trends in component costs (how they will change over time) is an important issue for designers
- Component prices drop over time without major improvements in manufacturing technology

What Affects Cost?

1. Learning curve:

- The more experience in manufacturing a component, the better the yield
- In general, a chip, board or system with twice the yield will have half the cost.
- The learning curve is different for different components, complicating design decisions

2. Volume

- Larger volume increases rate of learning curve
- Doubling the volume typically reduce cost by 10%

3. Commodities

- Are essentially identical products sold by multiple vendors in large volumes
- Foil the competition and drive the efficiency higher and thus the cost down