# CMSC 611: Advanced Computer Architecture

Compilers & ISA

### **Lecture Overview**

- Last week
  - Type and size of operands
    - (common data types, effect of operand size on complexity)
  - Encoding the instruction set
    - (Fixed, variable and hybrid encoding, stored program)
- This week
  - The role of the compiler
  - Effect of ISA on Compiler Complexity
  - Pipeline performance
  - Pipeline hazards

## **Typical Compilation**

#### Dependencies

Language dependent; machine independent

Front-end per language

Intermediate representation

High-level optimizations

#### Function

Transform language to common intermediate form

Somewhat language dependent, largely machine independent

Small language dependencies; machine dependencies slight (e.g., register counts/types) Global optimizer

Code generator

For example, procedure inlining and loop transformations

Including global and local optimizations + register allocation

Highly machine dependent; language independent Detailed instruction selection and machine-dependent optimizations; may include

## **Compiling Array Indexing**

Let's assume that A is an array of word-length integers and that the compiler has associated the variables g, h and i with the registers \$s1, \$s2 and \$s4. Let's assume that the starting address, or base address, of the array is in \$s3. The following is a possible compilation of a segment of a C program to MIPS assembly instructions:

$$g = h + A[i];$$

#### First convert word-index to byte-index:

```
add $t1, $s4, $s4 # Temp reg $t1 = 2 * i
add $t1, $t1, $t1 # Temp reg $t1 = 4 * i
```

To get the address of A[i], we need to add \$t1 to the base of A in \$s3:

```
add $t1, $t1, $s3 # $t1 = address of A[i] (4 * i + $s3)
```

Now we can use that address to load A[i] into a temporary register:

```
lw $t0, 0($t1) # Temporary register $t0 gets A[i]
```

#### Finally add *A[i]* to *h* and place the sum in *g*:

```
add $$1, $$2, $$10 # g = h + A[i]
```

Compiling if-then-else

Assuming the five variables f, g, h, i, and j correspond to the five registers \$s0 through \$s4, what is the compiled MIPS code for the following C if statement:

$$if (i == j) f = g + h; else f = g - h;$$

#### **MIPS:**

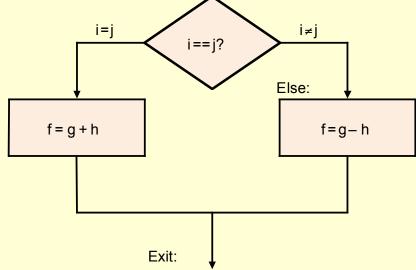
bne \$s3, \$s4, Else

add \$s0, \$s1, \$s2

j Exit

Else: sub \$s0, \$s1, \$s2

Exit:



# go to Else if i ≠ j

# f = g + h (skipped if  $i \neq j$ )

# f = g - h (skipped if i = j)

## Compiling a while Loop

Assume that i, j and k correspond to \$s3 through \$s5, and the base of the array "save" is in \$s6. what is the compiled MIPS code for the following C segment:

```
while (save[i] == k) i = i + j;
```

#### **MIPS:**

The first step is to load save[i] into a temporary register

```
Loop: add $t1, $s3, $s3  # Temp reg $t1 = 2 * i add $t1, $t1, $t1  # Temp reg $t1 = 4 * i add $t1, $t1, $s6  # $t1 = address of save[i] lw $t0, 0($t1)  # Temp reg $t0 = save[i]
```

The next instruction performs the loop test, exiting if save[i] ≠ k

```
bne $t0, $s5, Exit # go to Exit if save[i] ≠ k
```

The next instruction add j to i:

```
add $s3, $s3, $s4 #i = i + j
```

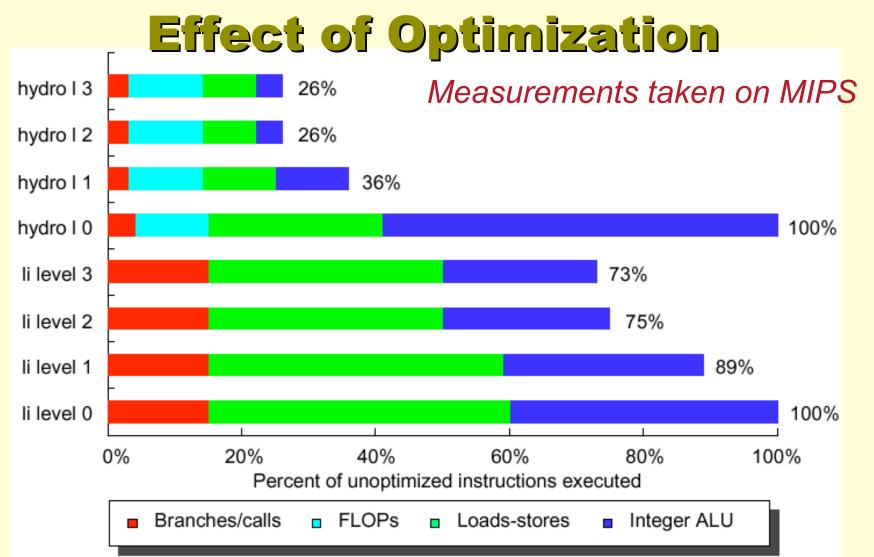
Finally reaching the loop end

```
j Loop # go back to the beginning of loop
```

Exit:

# **Major Types of Optimization**

<b>Optimization Name</b>	<b>Explanation</b>	<u>Frequency</u>
High -level	At or near source level; machine indep.	
Procedure integration	Replace procedure call by procedure body	N.M
Local	Within straight line code	
Common sub- expression elimination	Replace two instances of the same computation by single copy	18%
Constant propagation	Replace all instances of a variable that is assigned a constant with the constant	22%
Stack height reduction	Rearrange expression tree to minimize resources needed for expression evaluation	N.M
Global	Across a branch	
Global common sub expression elimination	Same as local, but this version crosses branches	13%
Copy propagation	Replace all instances of a variable A that has been assigned X (i.e., A = X) with X	11%
Code motion	Remove code from a loop that computes same value each iteration of the loop	16%
Induction variable elimination	Simplify/eliminate array –addressing calculations within loops	2%
Machine-dependant	Depends on machine knowledge	
Strength reduction	Many examples, such as replace multiply by a constant with adds and shifts	N.M
Pipeline Scheduling	Reorder instructions to improve pipeline performance	N.M.



Level 0: non-optimized code

**Level 2**: global optimization, s/w pipelining

Level 1: local optimization

<u>Level 3</u>: adds procedure integration

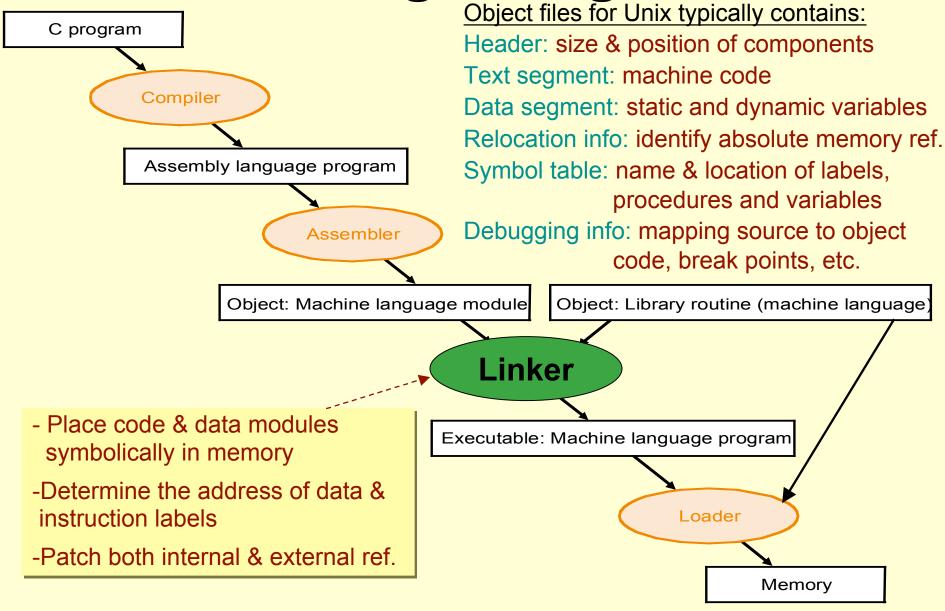
## **Multimedia Instructions**

- Small vector processing targeting multimedia
  - Intel's MMX, PowerPC AltiVec, Sparc VIS, MIPS MDMX
  - N 1/N<sup>th</sup>-word vectors packed into one register
  - Same operations performed on all N vectors
- Plus
  - Little additional ALU hardware
  - Utilize under-used hardware resources
- Minus
  - Extra pack & unpack if data isn't already arranged perfectly
  - Limited vector sizes, difficult to compile for general code
- Result
  - Mostly used in hand-coded libraries
- Compare to general vector processing
  - Hide memory latency in vector access
  - Strided processing, gather/scatter addressing

## Effect of Compilers on ISA

- Promote regularity
  - Limit # register formats and variability of operands
  - Orthogonality in operations, registers & addressing
- Provide primitives, not solutions
  - Common features over specific language features
  - Special-purpose instructions often unusable (except through hand-assembly-coded libraries)
- Simplify trade-offs among alternatives
  - Simplify the analysis of special features such as cache and pipeline
  - Allow simultaneous activities to promote optimization
- Favor static binding

Starting a Program



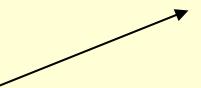
## **Linking Object Files**

Object file header			
,	Name	Procedure A	
	Text size	100 <sub>hex</sub>	
	Data size	20 <sub>hex</sub>	
Text segment	Address	Instruction	
	0	lw \$a0, 0(\$gp)	
	4	jal 0	
Data segment	0	(X)	
Relocation Info	Address	Instruction type	Dependency
	0	lw	X
	4	jal	В
Symbol table	Label	Address	
	X	-	
	В	-	

01: (5:1 1			
Object file header			
	Name	Procedure B	
	Text size	200 <sub>hex</sub>	
	Data size	30 <sub>hex</sub>	
Text segment	Address	Instruction	
	0	lw \$a0, 0(\$gp)	
	4	jal <mark>0</mark>	
Data segment	0	( <b>Y</b> )	
Relocation Info	Address	Instruction type	Dependency
	0	lw	Υ
	4	jal	Α
Symbol table	Label	Address	
	Υ	-	
	Α	-	

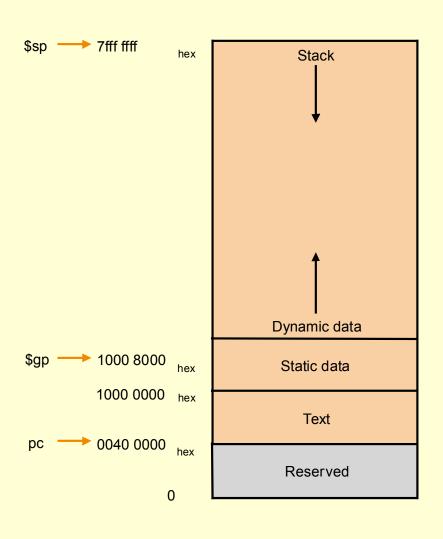


Executable file header		
	Text size	300 <sub>hex</sub>
	Data size	50 <sub>hex</sub>
Text segment	Address	Instruction
	0040 0000 <sub>hex</sub>	lw \$a0, 8000 <sub>hex</sub> (\$gp)
	0040 0004 <sub>hex</sub>	jal 40 0100 <sub>hex</sub>
	•••	•••
	0040 0100 <sub>hex</sub>	lw \$a1, 8020 <sub>hex</sub> (\$gp)
	0040 0104 <sub>hex</sub>	jal 40 0000 <sub>hex</sub>
Data segment	Address	
	1000 0000 <sub>hex</sub>	( <b>X</b> )
		•••
	1000 0020 <sub>hex</sub>	(Y)



Assuming the value in \$gp is  $1000 8000_{\text{hex}}$ 

## Loading Executable Program



- To load an executable, the operating system follows these steps:
  - Read the executable file header to determine the size of text and data segments
  - 2. Create an address space large enough for the text and data
  - Copy the instructions and data from the executable file into memory
  - 4. Copy the parameters (if any) to the main program onto the stack
  - Initialize the machine registers and sets the stack pointer to the first free location
  - 6. Jump to a start-up routines that copies the parameters into the argument registers and calls the main routine of the program