Prognosis of NBTI Aging Using a Machine Learning Scheme

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***Abstract*—Circuit aging is an important failure mechanism in nanoscale designs and is a growing concern for the reliability of future systems. Aging results in circuit performance degradation over time and the ultimate circuit failure. Among aging mechanisms, Negative-Bias Temperature Instability (NBTI) is the main limiting factor of circuits lifetime. Estimating the effect of aging-related degradation, before it actually occurs, is crucial for developing aging prevention/mitigations actions to avoid circuit failures. In this paper, we propose a general-purpose IC aging prognosis approach by considering a comprehensive set of IC operating conditions including workload, usage time and operating temperature. In addition, our model considers process variation by using a calibration technique applied at the time of manufacturing. Experimental results confirms that our model is able to accurately predict the NBTI-related path delay degradation under various operating conditions. The proposed model is robust to process variations.**

I. Introduction

As aggressive scaling continues to push technology into smaller feature sizes, various design robustness concerns continue to arise. Among them, degradation mechanisms such as Negative-Bias Temperature-Instability (NBTI), Hot-Carrier Injection (HCI), and gate Oxide Breakdown (OB) have attracted enormous attention [1]–[3]. In practice, in advanced technologies, electrical behavior of transistors eventually deviates from its original intended behavior. This deviation may degrade performance; and consequently, the chip suddenly fails to meet some of the required specifications [4], [5].

Performance degradation of an IC due to aging is influenced by the operating conditions of the circuit including temperature, voltage bias, and current density [6]. In particular, among aging mechanisms, NBTI has received the lion's share of attention [7]. NBTI occurs when traps are generated at the Si-SiO_2 interface when a negative voltage is applied to a PMOS device [8]. It shifts the threshold voltage of the device during its lifetime, degrades the device drive current, and in turn degrades the circuit performance [9]. Although tremendous efforts have been invested to mitigate the aging effects, the effect of NBTI is still significant. In practice, as VLSI technology scales, NBTI significantly contributes in degrading circuit reliability [10], [11]. To mitigate NBTI-related performance degradation and to increase the reliability of circuits, several methods have been proposed in literature. Guard-banding, gate-sizing, voltage tuning (changing V_{dd} and V_{th}), and body biasing are among the methods used in industry to reduce the rate of timing and functional errors induced by NBTI effects [12].

The effect of aging mechanisms can be analyzed and monitored at real time to project aging degradation in a circuit in a foreseeable future [13]. This method, so called aging prognosis, allows to proactively estimate the effect of degradation before it actually occurs, such that preventive actions can be put in place to avoid catastrophic consequences. In predicting aging induced degradations, a number of environmental factors should be considered, including workload, temperature, voltage variations, process variation, etc [14].

In this paper, we propose a general-purpose IC aging prognosis approach by taking into account a comprehensive set of IC operating conditions including workload, usage time, run-time temperature, etc. We show that the impact of IC aging on critical path delays can be accurately predicted using non-linear regression models. Moreover, we generalize our prediction model for circuits under process variation using a calibration technique applied at the time of manufacturing. Thus, the effect of process variation on aging prediction can be compensated.

The rest of this paper is organized as follows. Section II presents a background on NBTI aging. Section III discusses the proposed aging prognosis method. Experimental Results and discussions are presented in Section IV. Conclusions and future directions are drawn in Section V.

II. Background on NBTI aging

NBTI is one of the leading factors in performance degradation of digital circuits. In practice, a PMOS transistor experiences two phases of NBTI depending on its bias condition. The first phase, i.e., the stress phase, occurs when the transistor is on, i.e., when a negative voltage is applied to its gate. In the stress phase, positive interface traps are generated at the Si-SiO_2 interface. As a result, the magnitude of the threshold voltage of the transistor is increased. In the second phase, i.e., recovery phase, a positive voltage is applied to the gate of the transistor. In this phase, the threshold voltage drift induced by NBTI during the stress phase can partially "recover".

Threshold voltage drifts of a PMOS transistor under stress depend on the physical parameters of the transistor, supply voltage, temperature, and stress time. Figure 1 shows the threshold voltage drift of a PMOS transistor that is continuously under stress for 6 months as well as a transistor that is under stress and recovery every other month. As shown, the NBTI effect is high in the first couple of months but the threshold voltage tends to saturate for long stress times.

In this paper, to evaluate the impact of NBTI on the performance of a circuit under stress, Synopsys HSpice MOSRA (MOS Reliability Analysis) [15] is deployed.

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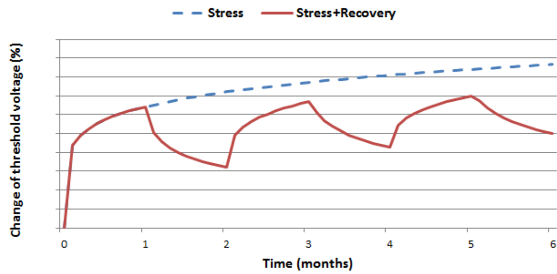

Fig. 1: Percentage change in threshold voltage of a PMOS transistor over time.

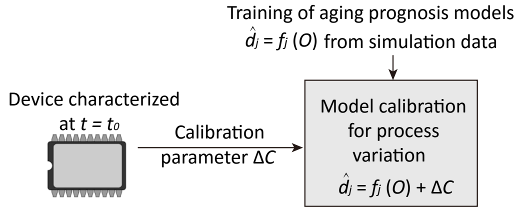

Fig. 2: Flowchart of the proposed aging prognosis approach

III. Proposed approach

In our aging prognosis model we consider a set of paths which if degraded by 20% due to aging would possibly cause failure. In this paper, we recall these paths as critical paths. The other paths do not mainly have the possibility of aging-related timing failures due to their short delay compared to this set of critical paths. Our proposed aging prognosis approach is based on training of non-linear regression models that map various circuit operating conditions to delays of critical paths. Moreover, we propose a calibration technique to compensate the effect of process variations on our path delay prediction. An overview of the proposed approach is summarized in Figure 2. What follows discusses the proposed approach in details.

A. Aging prognosis of nominal circuits under constant operating condition

To formulate the considered problem, let $O = [o_1, \ldots, o_n]$ denote the set of operating conditions under which the circuit operates, where n is the total number of considered operating conditions. We first consider the case for a nominal circuit without process variation under constant operating conditions, i.e., O is constant over time. Here, the delay of the j-th path of the nominal circuit (d_j) can be modeled by training a non-linear regression function mapping operating condition vector O to d_j. In particular, we train m regression functions: $f_j : O \mapsto d_j$, $j = 1, \ldots, m$, where m is the total number of considered critical paths in the circuit. The main goal is to construct regression models with generalization capabilities that can accurately predict aging for any given operating condition. In this work, we use multivariate adaptive regression splines (MARS) regression models for building f_j.

B. Aging prognosis of circuits under process variations and constant operating condition

The regression functions shown in the previous section aim at predicting aging of a nominal circuit under constant operating condition. However, circuits' path delays are subject to random variations during manufacturing. In this paper, we propose a simple calibration technique to compensate the effect of process variations at time $t = t_0$, such that the deviation of a circuit under process variations from a nominal circuit is compensated in aging prognosis.

Our calibration technique consists of 3 steps as below:

1) Performing the corner simulation to obtain the best/worst delay of all critical paths;
2) Computation of compensation factor of a new device under nominal operating condition at time $t = t_0$;
3) Process variation calibration using compensation factor computed in step 2.

Specifically, we propose to learn the model f_j, $j = 1, \ldots, m$ described in Section III-A for the best/worst corner cases. The best/worst models are denoted by $f_{j,min}$ and $f_{j,max}$, which are learned from best/worst corner circuit sampled at various operating condition O.

The second step of our aging prognosis for circuits under process variations is to compute the compensation factor for a manufactured circuit at time $t = t_0$. For any new fabricated circuits, we first need to measure its path delays at nominal operating condition denoted by O_{nom}. The delay of the j-th critical path at t_0 is denoted by $d_{j,n}$, where n denotes the nominal delay. Then using the corner models $f_{j,min}$ and $f_{j,max}$ learned from step 1, we can predict the j-th best/worst path delay values at t_0 and operating condition O_{nom}: $d_{j,min} = f_{j,min}(O_{nom})$, $d_{j,max} = f_{j,max}(O_{nom})$, $j = 1, \ldots, m$. Based on the above definitions, we define the process variation compensation scaling factor s_f as follows:

$$s_f = (d_{j,n} - d_{j,min})/(d_{j,max} - d_{j,min}) \quad (1)$$

In practice, the factor s_f defined above allows us to calibrate the circuit and compensate the impact of process variations on aging prediction at time $t = t_0$. Once s_f is computed, we can use it to calibrate new aging degradation predictions. Let $\hat{d}_j$ denote the predicted j-th path delay of a nominal circuit under consideration, as shown in Section III-A, we can then calibrate the aging prediction for any new circuit with s_f as compensation factor under operating condition O:

$$\hat{d}_{j,n} = d_{jo,min} + (d_{jo,max} - d_{jo,min}) \times s_f \quad (2)$$

where $d_{jo,min}/d_{jo,max}$ denote the best/worst predicted path delays under the operating condition O. Note that the same scaling factor s_f is used to compute the predicted path delay for any given operating condition O.

IV. Experimental results and Analysis

A. Experimental Setup

To evaluate the effectiveness of the proposed aging prognosis schemes, we used five ISCAS'89 benchmark circuits. Synopsys Design Compiler tool was used for logic synthesis

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at 45-nm technology using the open-source Nangate library [16]. Synopsys PrimeTime was used for extracting the timing-critical paths. They are obtained by selecting paths whose delay if degraded by 20% during the course of aging would possibly cause failure. HSpice MOSRA was used to conduct simulations and evaluate the effect of NBTI aging.

For each benchmark circuit, the HSpice simulations were performed for different workload and temperature scenarios. In particular, the operating temperature of $25°C$, $50°C$, and $75°C$ were considered. For each benchmark circuit, 5 workloads were generated such that in each workload, X% of the primary inputs got the value of '1' in each clock cycle, where X was 1%, 25%, 50%, 75%, or 99%. Using HSpice MOSRA, the effect of aging was evaluated for 8 years of circuit operation in time steps of 2 months.

To determine the effect of process variation in the proposed prognosis algorithm, we ran HSpice Monte Carlo (MC) simulations for each benchmark circuit using the following process-variation parameters for a Gaussian distribution: transistor gate length L: $3\sigma = 10\%$; threshold voltage V_{TH}: $3\sigma = 30\%$, and gate-oxide thickness t_{OX}: $3\sigma = 3\%$.

B. Experimental Results

1) Aging prognosis of nominal circuit under constant operating condition: We first evaluated aging prognosis model for nominal devices under constant operating conditions, as discussed in Section III-A. We have considered 3 operation conditions in our study, namely temperature T and duty cycle parameters α_1 and α_2 applied to the inputs of the first gate in a critical path. By combining with the usage time parameter t, our operating vector can be denoted by $O = [T, \alpha_1, \alpha_2, t]$. We have employed a Latin Hypercube Sampling (LHS) method to generate a total number of 2,000 samples in the space of operating condition vector O for model training and validation. The sampling ranges for the variables in O during LHS generation are: $T = [25, 75], \alpha_1, \alpha_2 = [0, 1], t = [0, 8yrs]$. We have performed aging simulation for each of the generated sample. Thus, the data set used for training and validation of the j-th critical path can be denoted by $S = [O^{(i)}, d^{(i)}], i = 1, \cdots, 2000$, where i denotes the sample index in the data set.

We then randomly split our data set into two equal subsets $S_{tr} = [O^{(i)}, d^{(i)}], i = 1, \cdots, 1000$ and $S_{val} = [O^{(i)}, d^{(i)}], i = 1001, \cdots, 2000$ for training and validation of our model. As discussed before, we used MARS regression models to learn the non-linear regression functions using S_{tr} that map operating condition vector O to j-th critical path delay : $f_j : O \mapsto d_j, j = 1, \ldots, m$, where m is the total number of considered critical paths, as shown in the second column of Table I. Once the model f_j is trained for each critical path, we use it to predict the delay of critical paths in the validation set S_{val} using $O^{(i)}, i = 1001, \cdots, 2000$ as inputs. The 3rd column in Table I shows the mean prediction error averaged over all 1000 samples in the validation set and all considered critical paths for each benchmark. As shown, our models are able to accurately predict delay values of all critical paths under *arbitrary* operating conditions.

To gain some insights on the path delay prediction, Figure 3 shows the sorted error plot of all the 392 critical paths for s5378 benchmark. As can be observed, the mean errors of most critical paths are under 4%, which shows excellent prediction results. Figure 4 shows prediction scatter plots for the two path delays with smallest prediction errors, as well as the two with highest prediction errors in s5378. As can be observed, even in the worst case, the prediction scatter plots follow the 45-degree line with the mean prediction error still below 5%.

2) Aging prognosis of circuits under process variations and constant operating condition: To evaluate the effectiveness of our approach in predicting path delays for circuits under process variation, we have i) manually selected K samples in $[T, \alpha_1, \alpha_2]$ and ii) for each of the K samples, generated

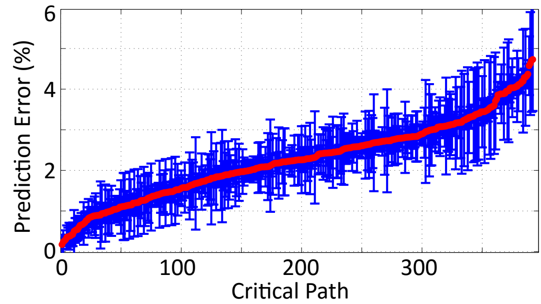

Fig. 3: Error plot for s5378 benchmark

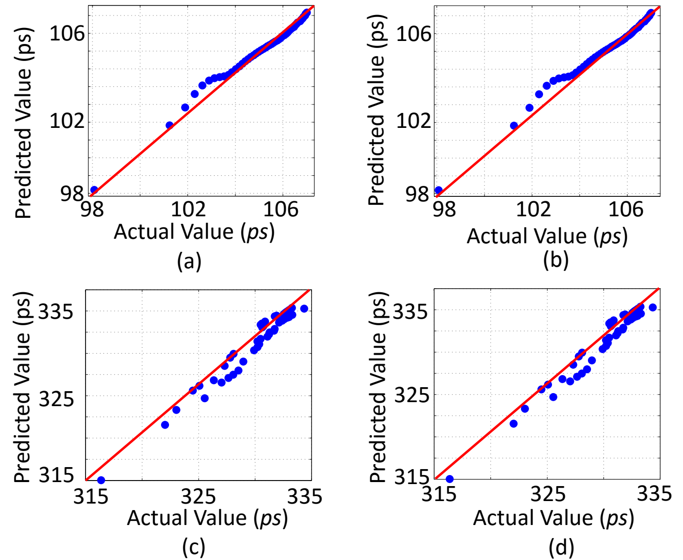

Fig. 4: Scatter plot for path delay prediction of s5378: (a)(b) the two best delay predictions of path 181 and 242 (c)(d) the two worst delay predictions of path 245 and 246

TABLE I: Aging prediction results for nominal devices under constant operating conditions

Benchmark	# of considered critical paths	Mean prediction error
s510	21	2.5%
s1494	57	2.43%
s5378	392	2.51%
s9234	179	2.67%
s15850	180	2.65%

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TABLE II: Aging prediction results for devices under process variations and constant operating conditions

Benchmark	# of considered critical paths	Mean prediction error
s510	21	2.62%
s1494	57	2.57%
s5378	392	2.62%
s9234	179	2.83%
s15850	180	3.15%

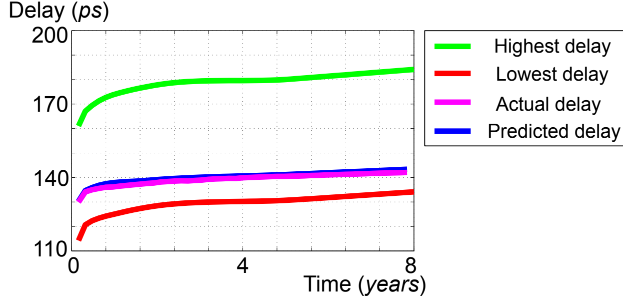

Fig. 5: Example of prediction of path delay under process variations for s5378

aging profile of 5 path delay samples from MC simulation, as well as the aging profile of nominal circuits. The aging profile consists of 49 path delay values equally sampled between 0 and 8 years in an aging simulation. We have considered 3 temperature values: 25, 50, 75 and 5 pairs of equal α_1 and α_2 values: 0.1, 0.25, 0.5, 0.75, 0.99. The combinations of these 2 sets gives us $K = 3 \times 5 = 15$ samples. For each of these samples, we first perform 5 MC simulations to obtain the process parameters, which will then be used to generate aging profiles as described. In addition to the 5 MC aging profiles, we generated corner aging profiles as described in Section III-B. The green/red curve in Figure 5 show the aging profile of the highest/lowest delay for a critical path in s5378, obtained using one of the previously mentioned K samples.

We used the calibration method described in Section III-B to make our prognosis prediction for the 5 generated aging profiles for each of the considered critical path. The 3rd column of Table II summarizes the averaged prediction errors for all benchmarks computed over all time points in the $K = 15$ aging profiles, each of which contains 5 MC samples. As shown, the averaged prediction errors are still maintained very low. As an example, the purple curve in Figure 5 shows the aging profile of a randomly selected critical path in benchmark s5378, sampled using one of the $K = 15$ operating samples in $[T, \alpha_1, \alpha_2]$, and generated from MC simulation. The blue curve shows the predicted aging profile using our approach. As shown, these two curves almost overlap with each other, confirming an excellent capability of the proposed approach to predict path delays of devices under process variations.

V. Conclusion

This paper presented an IC aging prognosis scheme that can be used to predict aging effects and take preventing actions before a circuit experiences aging-related malfunctions. The proposed machine-learning based scheme uses a comprehensive set of IC operating conditions including workload, usage time, and run-time temperature to train the model. We improved our prediction model and considered the effect of process variations in the aging prognosis process. The experimental results showed that the impact of IC aging on critical path delays can be accurately predicted using our non-linear regression models. Our future plans include stress testing of a complex circuit with realistic time-varying operating conditions by considering dynamic modeling of temperature and workload variations.

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