NAGHMEH KARIMI

CONTACT INFORMATION
1000 Hilltop Circle, ITE 314
Baltimore, MD 21250

E-mail: nkarimi@umbc.edu
Web: http://csee.umbc.edu/~nkarimi/
Phone: 646-831-9917

CURRENT POSITION
Assistant Professor
Department of Computer Science and Electrical Engineering
University of Maryland, Baltimore County (UMBC)

RESEARCH INTERESTS
- Hardware Security and Design-for-Trust
- Fault Tolerance and Design-for-Reliability
- VLSI Testing and Design-for-Testability
- VLSI and Electronic Circuits
- Computer Aided Design
- Internet of Things

EDUCATION

University of Tehran, Tehran, Iran 09/2002 - 02/2010
Ph.D. in Electrical Engineering
- Advisor: Prof. Zainalabedin Navabi (also at Worcester Polytechnic Inst.)
- Co-advisors: Prof. Yiorgos Makris (at Yale Univ. then) & Prof. Mehdi Sedighi
- Thesis: Concurrent Self-Testing of SoCs at Component Level

University of Tehran, Tehran, Iran 09/1999 - 09/2002
M.Sc. in Hardware Computer Engineering
- Advisor: Prof. Zainalabedin Navabi
- Co-advisor: Prof. Mehrdad Nourani (at Univ. Texas at Dallas)
- Thesis: Automatic Testability Enhancement in RTL Domain

University of Tehran, Tehran, Iran 09/1993 - 09/1997
B.Sc. in Hardware Computer Engineering

RESEARCH EXPERIENCE IN HIGHER EDUCATION

University of Maryland, Baltimore County, Baltimore, MD 01/2017 - present
Assistant Professor
- Hardware Security, Reliability, and Testing

Rutgers University, Piscataway , NJ 09/2014 - 12/2016
Visiting/Teaching Assistant Professor
- Research in Hardware Security and Reliability

New York University, New York , NY 09/2012 - 08/2014
Visiting Assistant Professor
- Research in Hardware Security and Reliability

New York University, New York , NY 02/2012 - 08/2012
Postdoctoral Re searcher with Prof. Ramesh Karri
- Research in Hardware Security

Duke University, Durham , NC 02/2011 - 01/2012
Postdoctoral Researcher with Prof. Krishnendu Chakrabarty
- Recovery from Clock-Domain Crossing Failures in Multi-Clock SoCs

Yale University, New Haven , CT 07/2007 - 07/2009
Visiting Research Assistant with Prof. Yiorgos Makris
- Concurrent Testing in Modern Microprocessors

University of Tehran, Tehran, Iran 09/1999 - 07/2007
Research Assistant with Prof. Zainalabedin Navabi
- Testability Enhancement and Concurrent Testing in Network-on-Chips

Teaching Experience in Higher Education

University of Maryland, Baltimore County, Baltimore, MA 2017-present
Instructor for:
- *"Hardware Security and Trust" (Grad & Undergrad)*
- *"VLSI Design Verification & Testing" (Grad & Undergrad)*
- *"Programmable Logic Devices" (Undergrad)*

Rutgers University, Piscataway, NJ 2014-16
Instructor for:
- *"Testing of VLSI Circuits" (Grad & Undergrad)*
- *"VLSI Design" (Grad & Undergrad)*
- *"Computer Architecture" (Grad)*
- *"Computer Architecture & Assembly Language" (Undergrad)*

New York University, New York, NY 2012-14
Instructor for:
- *"VLSI System Testing" (Grad)*
- *"Introduction to VLSI Design" (Grad & Undergrad)*

Yale University, New Haven, CT 2009
- *Teaching Assistant for "VLSI Testing" (Grad)*

University of Tehran, Tehran, Iran 2003-06
- *Instructor for "Graph Theory" and "Discrete Mathematics"*

University of Tehran, Tehran, Iran 2002
- *Teaching Assistant for "VHDL Hardware Description Language"*

Honors Received

- **2nd Place of Digital Trust Competition** 2022
  INCS-CoE – InterNational Cyber Security Center of Excellence
- **2nd Place of Hardware Demo Competition** 2022
  (my Ph.D. students), IEEE Hardware-Oriented Security and Trust Symp. (HOST)
- **Faculty Early Career Development (CAREER) Award**, NSF 2020
- **2nd Place of Embedded Security Challenge Competition** 2018
  (my Ph.D. students), Annual competition held in NYU
- **1st Place of Innovation Award**, Capstone Project, ECE, Rutgers University 2016
  (my Undergrad students)
- **Visiting Faculty Fellowship**, New York University 2012-14
- **Postdoctoral Scholarship**, VLSI Testing Lab, Duke University 2011-12
- **Travel Grant**, Young Faculty Workshop in Design Automation Conf. (DAC) 2012
- **Travel Grant** Workshop on Diversity on Design Automation and Test (WD2AT) 2011
- **Ph.D. Thesis Award**, Iran Nanotechnology initiative council 2010
- **Visiting Assistant in Research Scholarship**, TRELA Lab, Yale University 2007-09
- **Travel Grant** Ph.D. Forum, Design Automation and Test in Europe Conf., (DATE) 2006
- **Ph.D. Research Award**, ECE Department, Univ. of Tehran 2006
- **1st Place of Ph.D. Entrance Exam**, Computer Eng., Univ. of Tehran 2002

Funding Support

External:

- Hardware-Assisted Trust Management Framework for Distributed IoT Applications — 2022-23
  Johns Hopkins University Applied Physics Laboratory (APL): $50,000
  Role: Co-PI (My share: **$25,000**)
- International Digital Trust Interoperability between US, UK, and Japan — 2022-23
  Int'l Cyber Security Center Of Excellence: **$5,500**
  Role: PI from UMBC
- Improving the interpretation of Deep Networks — 2022
  Northrop Grumman: **$75,000**
  Role: Sole PI
- Measuring and Improving the Robustness of Deep Learning Algorithms in the Presence of Adversary — 2022
  NIST: **$76,000**
  Role: Sole PI (Former PI: Hamed Pirsiavash)
- Investigating the Impact of Device Aging on the Security of Cryptographic Chips — 2020-25
  NSF CAREER Award: **$500,000**
  Role: Sole PI
- Wildly Corrupting Yet Hard-to-Break Hardware Obfuscation — 2020-21
  AFRL/Northrop Grumman: **$370,000**
  Received $170,000 due to the change of program at AFRL
  Role: PI from UMBC (Collaborative with GMU)
- Acquisition of a Heterogeneous GPU Cluster to Facilitate Deep Learning — 2019-22
  NSF MRI: **$300,000**
  Role: Co-PI
- Student travel support for IEEE VTS — 2018-19
  NSF CCF: **$12,000**
  Role: Sole PI

Internal:

- Side-Channel Leakage Analysis and Prevention — 2022-23
  UMBC SURE Grant: **$1,500**
  Role: Sole PI
- Acquisition of a Heterogeneous GPU Cluster to Facilitate Deep Learning — 2019-22
  Cost-sharing for NSF MRI: **$129,000**
  Role: Co-PI
- Security of Integrated Circuits' Supply Chain: Threats and Countermeasures — 2020-21
  STrategic Awards for Research Transitions (START): **$25,000**
  Role: Sole PI
- Addressing Stability and Aging Resiliency of Delay-PUFs, — 2017
  Summer Faculty Fellowship at UMBC: **$6,000**
  Role: Sole PI

Selected Publications

Book Chapters

1. N. Karimi, "Security and Device Aging," In *Encyclopedia of Cryptography, Security and Privacy*, 3rd Edition, to appear, Springer, USA, 2022.
2. N. Karimi and Z. Navabi, "VHDL-AMS Hardware Description Language," In *The VLSI Handbook*, 2nd Edition, Chapter 91, Section XIII, CRC Press, USA, 2006.

3. N. Karimi and Z. Navabi, "ASIC and Custom IC Cell Information Representation," In *The VLSI Handbook*, 2nd Edition, Chapter 93, Section XIII, CRC Press, USA, 2006.

4. N. Karimi and Z. Navabi, "Timing Description Languages," In *The VLSI Handbook*, 2nd Edition, Chapter 95, Section XIII, CRC Press, USA, 2006.

Journal Articles

1. T. Kroeger, W. Cheng, S. Guilley, J.-L. Danger, and N. Karimi, "Cross-PUF Attacks: Targeting FPGA Implementation of Arbiter-PUFs," *Springer Journal of Electronic Testing* (*JETTA*), vol. 38, no. 3, pp. 261-277, 2022.

2. T. Kroeger, W. Cheng, S. Guilley, J.-L. Danger, and N. Karimi, "Assessment and Mitigation of Power Side-Channel based Cross-PUF Attacks on Arbiter-PUFs and their Derivatives," *IEEE Trans. on Very Large Scale Integration Systems* (*TVLSI*), vol. 30, no. 2, pp. 187-200, 2022.

3. F. Niknia, J.-L. Danger, S. Guilley, and N Karimi, "Aging Effects on Template Attacks Launched on Dual-Rail Protected Chips," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 41, no. 5, pp. 1276-1289, 2022.

4. M. T. H. Anik*, M. Ebrahimabadi*, J.-L. Danger, S. Guilley, and N. Karimi, "Reducing Aging Impacts in Digital Sensors via Run-time Calibration, " *Springer Journal of Electronic Testing* (*JETTA*), vol. 37, no. 5-6, pp. 653-673, 2022 *equal contribution.

5. W. Lalouani, M. Younis, M. Ebrahimabadi, and N. Karimi, "Countering Modeling Attacks in PUF-based IoT Security Solutions," *ACM Journal on Emerging Technologies in Computing Systems* (*JETC*), vol. 18, no. 3, pp.46:1-46:28, 2022.

6. M. Ebrahimabadi, M. Younis, and N. Karimi, "A PUF-Based Modeling-Attack Resilient Authentication," *IEEE Internet of Things (IoT) Journal*, vol. 9, no. 5, pp. 3684-3703, 2022.

7. B. Fadaeinia, M. T. H. Anik, N. Karimi, and A. Moradi, "Masked SABL: A Long Lasting Side-Channel Protection Design Methodology,", *IEEE Access*, vol. 9, pp. 90455-90464, 2021.

8. A. Vakil, A. Mirzaeian, H. Homayoun, N. Karimi, and A. Sasan, "AVATAR: NN-Assisted Variation Aware Timing Analysis and Reporting for Hardware Trojan Detection," *IEEE Access*, vol. 9, pp.92881-92900, 2021.

9. N. Karimi, K. Basu, C.-H. Chang, and J. M. Fung, "Hardware Security in Emerging Technologies: Vulnerabilities, Attacks, and Solutions," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (*JETCAS*), vol. 11, no. 2, pp. 223-227, 2021.

10. W. Liu, C.-H. Chang, X. Wang, C. Liu, J. M. Fung, M. Ebrahimabadi, N. Karimi, X. Meng, and K. Basu, "Two Sides of the Same Coin: Boons and Banes of Machine Learning in Hardware Security," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (*JETCAS*), vol. 11, no. 2, pp. 228-251, 2021.

11. M. T. H. Anik, J.-L. Danger, S. Guilley, and N. Karimi, "Detecting Failures and Attacks via Digital Sensors", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), pp. 1315-1326, 2021.

12. N. Karimi, T. Moos, and A. Moradi, "Exploring the Effect of Device Aging on Static Power Analysis Attacks," *IACR Trans. on Cryptographic Hardware and Embedded Systems* (*CHES*), pp. 233-256, 2019.

13. J. Shey, N. Karimi, R. Robucci, and C. Patel, "Implementation-Based Design Fingerprinting for Robust IC Fraud Detection," *Journal of Hardware and Systems security*, vol. 3, no. 4, pp. 426-439, 2019.

14. K. Huang, X. Zhang, and N. Karimi, "Real-Time Prediction for IC Aging based on Machine Learning," *IEEE Trans. on Instrumentation and Measurement* (*TIM*), vol. 68, nO. 12, PP. 4756-4764, 2019.

15. N. Karimi, J. Danger, and S. Guilley, "Impact of Aging on the Reliability of Delay PUFs," *Springer Journal of Electronic Testing: Theory and Applications* (*JETTA*), vol. 34, no. 5, pp.571-586, 2018.

16. N. Karimi, A. Kanuparthi, X. Wang, O. Sinanoglu, and R. Karri, "MAGIC: Malicious Aging in Circuits/Cores," ACM Trans. on *Architecture and Code Optimization* (*TACO*), vol. 12, pp. 5.1-5.25, 2015.

17. S. Kannan, N. Karimi, O. Sinanoglu, and R. Karri, "Security Vulnerability of Emerging Non-Volatile Main Memories and Countermeasures," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 34, no. 1, pp. 2-15, 2015.

18. S. Kannan, N. Karimi, R. Karri, and O. Sinanoglu, "Modeling, Detection, and Diagnosis of Faults in Multi-Level Memristor Memories," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol.34, no.5, pp. 822-834, 2015.

19. A. DeTrano, N. Karimi, R. Karri, X. Guo, C. Carlet, S. Guilley, "Exploiting Small Leakages in Masks to Turn a Second-Order Attack into a First-Order Attack and Improved Rotating Substitution Box Masking with Linear Code Cosets," *The Scientific World Journal*, vol. 2015, pp. 1-10, 2015.

20. N. Karimi and K. Chakrabarty, "Detection, Diagnosis and Recovery from Clock-Domain Crossing Failures in Multi-Clock SoCs," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* (*TCAD*), vol. 32, no. 9, pp. 1395-1408, 2013.

21. N. Karimi, M. Maniatakos, C. Tirumurti, and Y. Makris, "On the Impact of Performance Faults in Modern Microprocessors," *Springer Journal of Electronic Testing: Theory and Applications* (*JETTA*), vol. 29, pp. 351-366, 2013.

22. N. Karimi, M. Maniatakos, A. Jas, C. Tirumurti, and Y. Makris, "Workload-Cognizant Concurrent Error Detection in the Scheduler of a Modern Microprocessor," *IEEE Trans. on Computers* (*TCOMP*), vol. 60, no. 9, pp. 1274-1287, 2011.

23. M. Maniatakos, N. Karimi, C. Tirumurti, A. Jas, and Y. Makris, "Instruction-Level Impact Analysis of Low-Level Faults in a Modern Microprocessor Controller," *IEEE Trans. on Computers* (*TCOMP*), vol. 60, no. 9, pp. 1260-1273, 2011.

24. N. Karimi, et al., "Online Network-on-Chip Switch Fault Detection and Diagnosis Using Functional Switch Faults," *Journal of Universal Computer Science* (*JUCS*), vol. 14, no. 22, pp. 3716-3736, 2008.

Conference Papers

1. S. Takarabt, J. Bahrami, M. Ebrahimabadi, S. Guilley, and N. Karimi, "Security Order of Gate-Level Masking Schemes," *Proc. IEEE IEEE Hardware-Oriented Security and Trust Symp.* (*HOST*), 2023, Accepted for publication.

2. M. Ebrahimabadi, M. Younis, W. Lalouani, A. Alshaeri, and N. Karimi, "SWeeT: Security Protocol for Wearables Embedded Devices' Data Transmission," *Proc. IEEE Int'l Conf. on E-health Networking, Application & Services* (*HEALTHCOM*), 2022.

3. W. Lalouani, M. Younis, M. Ebrahimabadi, and N. Karimi, "Collusion-resistant PUF-based Distributed Device Authentication Protocol for Internet of Things," *Proc. IEEE Global Communications Conference: IoT and Sensor Networks* (*GLOBECOM*), 2022.

4. J. Bahrami, M. Ebrahimabadi, J.-L. Danger, S. Guilley, and N. Karimi, "Leakage Power Analysis in Different S-Box Masking Protection Schemes," *Proc. IEEE Design Automation & Test in Europe* (*DATE*), 2022, pp. 1263-1268.

5. W. Lalouani, M. Younis, M. Ebrahimabadi, and N. Karimi, "Robust and Efficient Data Security Solution for Pervasive Data Sharing in IoT," Accepted for publication, *Proc. IEEE Consumer Communications & Networking Conference* (*CCNC*), 2022, pp. 775-781.

6. J. Bahrami, M. Ebrahimabadi, S. Takarabt, J.-L. Danger, S. Guilley, and N. Karimi, "On the Practicality of Relying on Simulations in Different Abstraction Levels for Pre-silicon Side-Channel Analysis," *Proc. Int'l Conf. on Security and Cryptography* (*SECRYPT*), 2022, pp. 661-668.

7. M Sadi, Y He, Y Li, M Alam, S Kundu, S Ghosh, J Bahrami, and N Karimi, "On the Reliability of Conventional and Quantum Neural Network Hardware, " *Proc. VLSI Test Symp.* (*VTS*), 2022.

8. M Ebrahimabadi, B Fadaeinia, A Moradi, and N Karimi, "Does Aging Matter? The Curious Case of Fault Sensitivity Analysis,", *Proc. Int'l Symp. on Quality Electronic Desig* (*ISQED*), 2022, pp. 84-89.

9. M Ebrahimabadi, S. S. Mehjabin, R Viera, S Guilley, J.-L. Danger, J.-L. Dutertre, N. Karimi, "Detecting Laser Fault Injection Attacks via Time-to-Digital Converter Sensors," *Proc. IEEE Hardware-Oriented Security and Trust Symp.* (*HOST*), pp. 97-100.

10. M Ebrahimabadi, M Younis, W Lalouani, and N Karimi, "An Attack Resilient PUF-based Authentication Mechanism for Distributed Systems,", *Proc. Int'l Conf. on VLSI Design and Embedded Systems* (*VLSID*), 2022, pp.1-6.

11. T. Kroeger, W. Cheng, S. Guilley, J.-L. Danger, and N. Karimi, "Making Obfuscated PUFs Secure Against Power Side-Channel Based Modeling Attacks," *Proc. IEEE Design Automation & Test in Europe Conf.* (*DATE*), 2021, pp. 454-459.

12. M. T. H. Anik, B. Fadaeinia, A. Moradi, and N. Karimi, "On the Impact of Aging on Power Analysis Attacks Targeting Power-Equalized Cryptographic Circuits," *Proc. IEEE Asia and South Pacific Design Automation Conference Conf.* (*ASP-DAC*), 2021, pp. 414-420.

13. A. Vakil, F. Niknia, A. Mirzaeian, A. Sasan, and N. Karimi, "Learning Assisted Side Channel Delay Test for Detection of Recycled ICs," *Proc. IEEE Asia and South Pacific Design Automation Conference Conf.* (*ASP-DAC*), 2021, pp. 455-462.

14. T. Kroeger, W. Cheng, S. Guilley, J.-L. Danger, and N. Karimi, "Enhancing the Resiliency of Multi-Bit Parallel Arbiter-PUF and its Derivatives against Power Attacks," *Int'l Workshop on Constructive Side-Channel Analysis and Secure Design* (*COSADE*), 2021, pp. 303-321.

15. K. Huang, M. T. H. Anik, X. Zhang, and N. Karimi, "Real-Time IC Aging Prediction via On-Chip Sensors," *Proc. IEEE Computer Society Annual Symp. on VLSI* (*ISVLSI*), 2021, pp. 13-18.

16. T. H. Anik, J.-L. Danger, O. Diankha , M. Ebrahimabadi, C. Frisch, S. Guilty, N Karimi, M. Pehl, and S. Takarabt,"Testing and Reliability Enhancement of Security Primitives," *Proc. IEEE Int'l Symp. on Defect and Fault Tolerance of VLSI Systems* (*DFTS*), 2021, pp. 1-8.

17. M. Ebrahimabadi, W. Lalouani, M. Younis, N. Karimi, "Countering PUF Modeling Attacks through Adversarial Machine Learning," *Proc. IEEE Computer Society Annual Symp. on VLSI* (*ISVLSI*), 2021, pp. 356-361.

18. M. Ebrahimabadi, M. Younis, N. Karimi, "Hardware Assisted Smart Grid Authentication," *IEEE Int'l Conf. on Communications* (*ICC*) 2021, pp. 1-6.

19. M. Ebrahimabadi, M. Younis, W. Lalouani, N. Karimi, "A Novel Modeling-Attack Resilient Arbiter-PUF Design," *Proc. IEEE Int'l Conf. on VLSI Design* (*VLSID*), 2021, pp. 123-128.

20. M. Ebrahimabadi, M. T. H. Anik, J.-L. Danger, S. Guilley, and N. Karimi, "Using Digital Sensors to Leverage Chips' Security," *IEEE Int'l Conf. on Physical Assurance and Inspection of Electronics* (*PAINE*), 2020, pp. 1-6.

21. T. Kroeger, W. Cheng, S. Guilley, J.-L. Danger, and N. Karimi, "Cross-PUF Attacks on Arbiter-PUFs through Their Power Side-Channel," *Proc. IEEE Int'l Test Conf.* (*ITC*), 2020, pp. 1-5.

22. T. Kroeger, W. Cheng, S. Guilley, J.-L. Danger, and N. Karimi, "Effect of Aging on PUF Modeling Attacks Based on Power Side-Channel Observations," *Proc. IEEE Design Automation & Test in Europe Conf.* (*DATE*), 2020, pp. 454-459.

23. M. T. H. Anik, S. Guilley, J.-L. Danger, and N. Karimi, "On the Effect of Aging on Digital Sensors," *Proc. IEEE Int'l Conf. on VLSI Design* (*VLSID*), 2020, pp. 189-194.

24. A. Alipour, V. Beroulle, B. Cambou, J.-L. Danger, G. Di Natale, D. Hely, S. Guilley, and N. Karimi, "PUF Enrollment and Life Cycle Management: Solutions and Perspectives for the Test Community," *Proc. IEEE European Test Symp.* (*ETS*), 2020, pp. 1-10.

25. M. T. H. Anik, R. Saini, J.-L. Danger, S. Guilley, and N. Karimi, "Failure and Attack Detection by Digital Sensors," *Proc. IEEE European Test Symp.* (*ETS*), 2020, pp. 1-2.

26. M. T. H. Anik, M. Ebrahimabadi, H. Pirsiavash, J.-L. Danger, S. Guilley, and N. Karimi, "On-Chip Voltage and Temperature Digital Sensor for Security, Reliability, and Portability," *Proc. IEEE Int'l. Conf. on Computer Design* (*ICCD*), 2020, pp. 1-4.

27. S. Roshanisefat, H. M. Kamali, K. Z. Azar, S. M. P. Dinakarrao, N. Karimi, H. Homayoun, and A. Sasan, "DFSSD: Deep Faults and Shallow State Duality, A Provably Strong Obfuscation Solution for Circuits with Restricted Access to Scan Chain," *Proc. IEEE VLSI Test Symp.* (*VTS*), 2020, pp.1-6.

28. A. Vakil, F. Behnia, A. Mirzaeian, H. Homayoun, N. Karimi, and A. Sasan, "LASCA: Learning Assisted Side Channel Delay Analysis for Hardware Trojan Detection,", *Proc. IEEE Int'l Symp. on Quality Electronic Design* (*ISQED*), 2020, pp. 40-45.

29. H. Salmani, M. Yasin, J. Rajendran, T. Hoque, S. Bhunia, N. Karimi, "Countering IP Security threats in Supply chain," *Proc. IEEE VLSI Test Symp.* (*VTS*), 2019, pp.1-9.

30. N. Karimi, S. Guilley, and J. Danger, "Impact of Aging on Template Attacks," *Proc. ACM Great Lakes Symp. on VLSI* (*GlSVLSI*), 2018, pp. 455-458.

31. N. Karimi, J. Danger, and S. Guilley, "On the Effect of Aging in Detecting Hardware Trojan Horses with Template Analysis," *Proc. IEEE Int'l Symp. on On-Line Testing and Robust System Design* (*IOLTS*), 2018, pp. 281-286.

32. J. Shey, N. Karimi, R. Robucci, and C. Patel, "Design-Based Fingerprinting Using Side-Channel Power Analysis for Protection Against IC Piracy," *Proc. IEEE Computer Society Annual Symp. on VLSI* (*ISVLSI*), 2018, pp. 614-619.

33. D.Kraak, M. Taouil, S. Hamdioui, P. Weckx, F. Catthoor, A. Singh, A. Chatterjee, H.-J.Wunderlich, and N. Karimi, "Device Aging: A Security and Reliability Concern," *Proc. IEEE European Test Symp.* (*ETS*), 2018, pp. 1-10.

34. N. Karimi, J. Danger, M. Slimani, and S. Guilley, "Impact of the Switching Activity on the Aging of Delay-PUFs," *Proc. IEEE European Test Symp.* (*ETS*), 2017, pp. 1-2.

35. N. Karimi, J. Danger, F. Lozac'h, and S. Guilley, "Predictive Aging of Reliability of two Delay PUFs," *Proc. Springer Int'l Conf. on Security, Privacy and Applied Cryptographic Engineering* (*SPACE*), 2016, pp. 213-232.

36. N. Karimi and K. Huang, "Prognosis of NBTI Aging Using a Machine Learning Scheme," *Proc. IEEE Int'l Symp. on Defect and Fault Tolerance of VLSI Systems* (*DFTS*), 2016, pp. 7-10.

37. X. Guo, N. Karimi, F. Regazzoni, C.Jin, and R. Karri "Simulation and Analysis of Negative-Bias Temperature Instability Aging on Power Analysis Attacks," *Proc. IEEE Hardware-Oriented Security and Trust Symp.* (*HOST*), 2015, pp. 124-129.

38. A. DeTrano, S. Guilley, X. Guo, N. Karimi, R. Karri, "Exploiting Small Leakages in Masks to Turn a Second-Order Attack into a First-Order Attack," *Proc. ACM Hardware and Architectural Support for Security and Privacy* (*HASP*), 2015, pp. 7:1-7:5.

39. S. Kannan, N. Karimi, and O. Sinanoglu, "Secure Memristor-Based Main Memory," *Proc. IEEE Design Automation Conf.* (*DAC*), 2014, pp.1-6.

40. S. Kannan, N. Karimi, R. Karri, and O. Sinanoglu, "Detection, Diagnosis, and Repair of Faults in Memristor-Based Memories," *Proc. IEEE VLSI Test Symp.* (*VTS*), 2014, pp.1-6.

41. O. Sinanoglu, N. Karimi, J. Rajendran, R. Karri, Y. Jin, K. Huang, and Y. Makris, "Reconciling the IC Test and Security Dichotomy," *Proc. IEEE European Test Symp.* (*ETS*), 2013, pp. 1-6.

42. N. Karimi, K. Chakrabarty, P. Gupta, and S. Patil, "Test Generation for Clock Domain Crossing Faults in Integrated Circuits," *Proc. IEEE Design Automation & Test in Europe Conf.* (*DATE*), 2012, pp. 406-411.

43. N. Karimi, Z. Kong, K. Chakrabarty, P. Gupta, and S. Patil, "Testing of Clock-Domain Crossing Faults in Multi-Core System-on-Chip," *Proc. IEEE Asian Test Symp.* (*ATS*), 2011, pp. 7-14.

44. N. Karimi, S. Sadeghi, and Z. Navabi, "Network-on-Chip Concurrent Error Recovery Using Functional Switch Faults," *Proc. IEEE Workshop on RTL and High Level Testing* (*WRTLT*), 2010.

45. N. Karimi, M. Maniatakos, C. Tirumurti, A. Jas, and Y. Makris, "Impact Analysis of Performance Faults in Modern Microprocessors," *Proc. IEEE Int'l. Conf. on Computer Design* (*ICCD*), 2009, pp. 91-96.

46. M. Maniatakos, N. Karimi, C. Tirumurti, A. Jas, and Y. Makris, "Instruction-Level Impact Comparison of RT- vs. Gate-Level Faults in a Modern Microprocessor Controller," *Proc. IEEE VLSI Test Symp.* (*VTS*), 2009, pp. 9-14.

47. N. Karimi, M. Maniatakos, Y. Makris, and A. Jas, "On the Correlation between Controller Faults and Instruction-Level Errors in Modern Microprocessors," *Proc. IEEE Int'l. Test Conf.* (*ITC*), 2008, pp. 24.1.1-24.1.10.

48. A. Alaghi, M. Sedghi, N. Karimi, and Z. Navabi, "NoC Reconfiguration for Utilizing the Largest Fault-Free Connected Sub-Structure," *Proc. IEEE Int'l. Test Conf.* (*ITC*), 2008, pp.1-1.

49. M. Maniatakos, N. Karimi, Y. Makris, A. Jas, and C. Tirumurti, "Design and Evaluation of a Timestamp-Based Concurrent Error Detection Method (CED) in a Modern Microprocessor Controller," *Proc. IEEE Int'l Symp. on Defect and Fault Tolerance of VLSI Systems* (DFTS), 2008, pp. 454-462.

50. A. Alaghi, M. Sedghi, N. Karimi, M. Fathy, and Z. Navabi, "Reliable NoC Architecture Utilizing a Robust Rerouting Algorithm," *Proc. IEEE Int'l East-West Design and Test Symp.* (*EWDTS*), 2008, pp. 200-203.

51. N. Karimi, S. Aminzadeh, S. Safari, and Z. Navabi, "A Novel GA-Based High-Level Synthesis Technique to Enhance RT-level Concurrent Testing," *Proc. IEEE Int'l. Online Test Symp.* (*IOLTS*), 2008, pp. 173-174.

52. A. Alaghi, N. Karimi, et al., "Online NoC Switch Fault Detection and Diagnosis Using a High Level Fault Model," *Proc. IEEE Int'l. Symp. on Defect and Fault Tolerance of VLSI Systems* (*DFTS*), 2007, pp. 21-30.

53. N. Karimi, S. Mirkhani, Z. Navabi, and F. Lombardi, "RT Level Reliability Enhancement by Constructing Dynamic TMRs," *Proc. ACM Great Lakes Symp. on VLSI* (*GlSVLSI*), 2007, pp. 172-175.

54. N. Karimi, and Z. Navabi, "A Dynamic Reconfiguration Method for Error Recovery of RT Level Designs," *Proc. IEEE Int'l. East-West Design and Test Symp.* (*EWDTS*), 2007, pp. 249-254.

55. N. Karimi, S. Mirkhani, and Z. Navabi, "ESTA: An Efficient Method for Reliability Enhancement of RT-Level Designs," *Proc. IEEE Asian Test Symp.* (*ATS*), 2006, pp. 195-202.

56. N. Karimi, P. Riahi, and Z. Navabi, "A Survey of Testability Measurements at Various Abstraction Levels," *Proc. IEEE North Atlantic Test Workshop* (*NATW*), 2003, pp. 26- 33.

57. P. Riahi, Z. Navabi, N. Karimi, and F. Lombardi, "A VPI-Based IP Core Serial Fault Simulation and Test Generation Methodology," *Proc. IEEE North Atlantic Test Workshop* (*NATW*), 2003, pp. 96-103.

Invited Talks & Tutorials

Invited Talk

- Does Device Aging Affect Security?
  IEEE Int'l Test Conf. -india (ITC-India) 2022
- Using Digital Sensors to Alleviate Chips' Security
  IEEE Int'l Conf. on Physical Assurance and Inspection of Electronics (PAINE) 2020
- Recent Developments in Hardware Security
  IEEE VLSI Test Symp. (VTS) 2018
- MAGIC: Malicious AGing In Circuits/Cores
  The Baltimore Chapter of IEEE Electron Devices & Solid-State Circuits 2017
- MAGIC: Malicious AGing In Circuits/Cores
  IEEE North Jersey Section, Jt Chapter, AP03/MTT17 2015

Panelist

- Women in Cyber Security: Past, Present and Future, WISE/HOST Symp. 2017

Tutorial

- Workshop for Women in Hardware and Systems Security (WISE) 2020

  Topic Title: Security and Aging: Friends or Foes?

Professional Service

Proposal Panel/Review

- NSF Panels 2019, 2020, 2021
- ARO Proposal Review 2017

Journal Editor

- IEEE Design and Test, Associate Editor, 2022-present
- Springer Journal of Electronic Testing: Theory and Applications (JETTA), Associate Editor, 2019-present
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS): Special issue of "Hardware Security in Emerging Technologies: Vulnerabilities, Attacks and Solutions", Guest Editor, 2020

Journal Reviewer

- IEEE Transactions on Computers (TCOMP)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Circuits and Systems I (TCAS)
- ACM Journal of Emerging Technologies in Computing (JETC)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- Springer Journal of Electronic Testing: Theory and Applications (JETTA)
- Elsevier Journal of Microprocessors and Microsystems - Embedded Hardware Design (MICPRO)
- IEEE Design & Test of Computers
- Canadian Journal of Electrical and Computer Engineering
- MDPI Journal of Cryptography

Conference Organizing Committee Member

- IEEE Hardware-Oriented Security and Trust Symp. (HOST), Tutorial Chair 2023
- IEEE Int'l Conf. on Omni-layer Intelligent systems (COINS), Program Chair 2021-23
- IEEE VLSI Test Symp. (VTS), Vice Program Chair 2022-23
- ACM Great Lakes Symp. on VLSI (GLSVLSI), Registration Chair 2023
- IEEE Dallas Circuits and Systems (DCAS), Publication Chair 2023
- IEEE VLSI Test Symp. (VTS), Special Session Chair 2021
- IEEE Hardware-Oriented Sec. & Trust Symp. (HOST), Ph.D. Thesis Competition Chair 2022
- ACM Workshop on Attacks and Solutions in Hardware Sec. (ASHES), Publicity Chair 2022
- IEEE Hardware-Oriented Security and Trust Symp. (HOST), Publicity Chair 2021-22
- ACM Great Lakes Symp. on VLSI (GLSVLSI), Publicity Chair 2021-22
- IEEE Int'l Symp. on Smart Electronic Systems (iSES), Publication Chair 2021
- IEEE VLSI Test Symp. (VTS), Chair of student activity 2017-20
- ACM Great Lakes Symp. on VLSI (GLSVLSI), Local Chair 2019
- WISE Workshop (in HOST Symp.), Poster Chair 2018-20

Conference Track Chair

- IEEE Symp. on Smart Electronic Systems (iSES) 2018
  Track of Hardware for Secure Information Processing
- ACM Great Lakes Symp. on VLSI (GLSVLSI) 2020-21
  Track of Hardware Security
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2022
  Track of Hardware Security

Conference Program Committee Member

- Int'l Conf. on Computer Aided Design (ICCAD) 2022-present
- Design Automation Conf. (DAC) 2021-present
- Conference on Cryptographic Hardware and Embedded Systems (CHES) 2020
- Hardware-Oriented Security and Trust Symp. (HOST) 2020-present
- IEEE Design and Test in Europe Conf. (DATE) 2019-present
- IEEE European Test Symp. (ETS) 2019-present
- IEEE Int'l Conf. on Consumer Electronics (ICCE) 2019
- IEEE Int'l Test Conf. (ITC) 2016-present
- IEEE Asian Test Symp. (ATS) 2016-19
- IEEE Asian Hardware Oriented Security and Trust Symp. (ASIAN HOST) 2017-19
- IEEE Int'l Conf. on VLSI Design (VLSID) 2016-19, 2022
- IEEE Great Lakes Symposium on VLSI (GLSVLSI) 2017-present
- IEEE North Atlantic Test Workshop (NATW) 2015-18
- IEEE Symp. on Defect & Fault Tolerance in VLSI Sys. (DFTS) 2014-present
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2014-present

Hot Topic Session Organizer

- IEEE VLSI Test Symp. (VTS) 2022
  Enhancing the Reliability of Neural Network accelerators
- IEEE VLSI Test Symp. (VTS) 2019
  Countering IP Security Threats in Supply Chain
- IEEE European Test Symp. (ETS) 2018
  Device Aging: A security and Reliability Concern

Judge for Best Hardware-Demo/Paper Award

- IEEE Hardware Oriented Security and Trust (HOST), Hardware Demo 2018-19
- IEEE European Test Symp. (ETS) 2020
- IEEE VLSI Test Symp. (VTS) 2020-21
- IEEE Symp. on Defect & Fault Tolerance in VLSI Sys. (DFTS) 2016
- IEEE Symp. on NanoScale Architectures (NANOARCH) 2013

Session Chair

- Design Automation and Test in Europe (DATE 2019, 2021)
- IEEE VLSI Test Symp. (VTS 2014, 2017, 2019, 2022)
- IEEE Hardware Oriented Security and Trust (HOST 2018)
- IEEE European Test Symp. (ETS 2018)
- Int'l Test Conf. (ITC 2015, 2017, 2018)
- IEEE Symp. on Defect and Fault Tolerance in VLSI and Nanotech. Sys. (DFTS 2013)
- IEEE/ACM Int'l Symp. on NanoScale Architectures (NANOARCH 2013)
- Workshop on Trustworthy Hardware (2013)