CMSC 313
COMPUTER ORGANIZATION
&
ASSEMBLY LANGUAGE PROGRAMMING

LECTURE 23, FALL 2012

TOPICS TODAY

- **Sequential Circuits**
- **Flip Flops**

SEQUENTIAL CIRCUITS

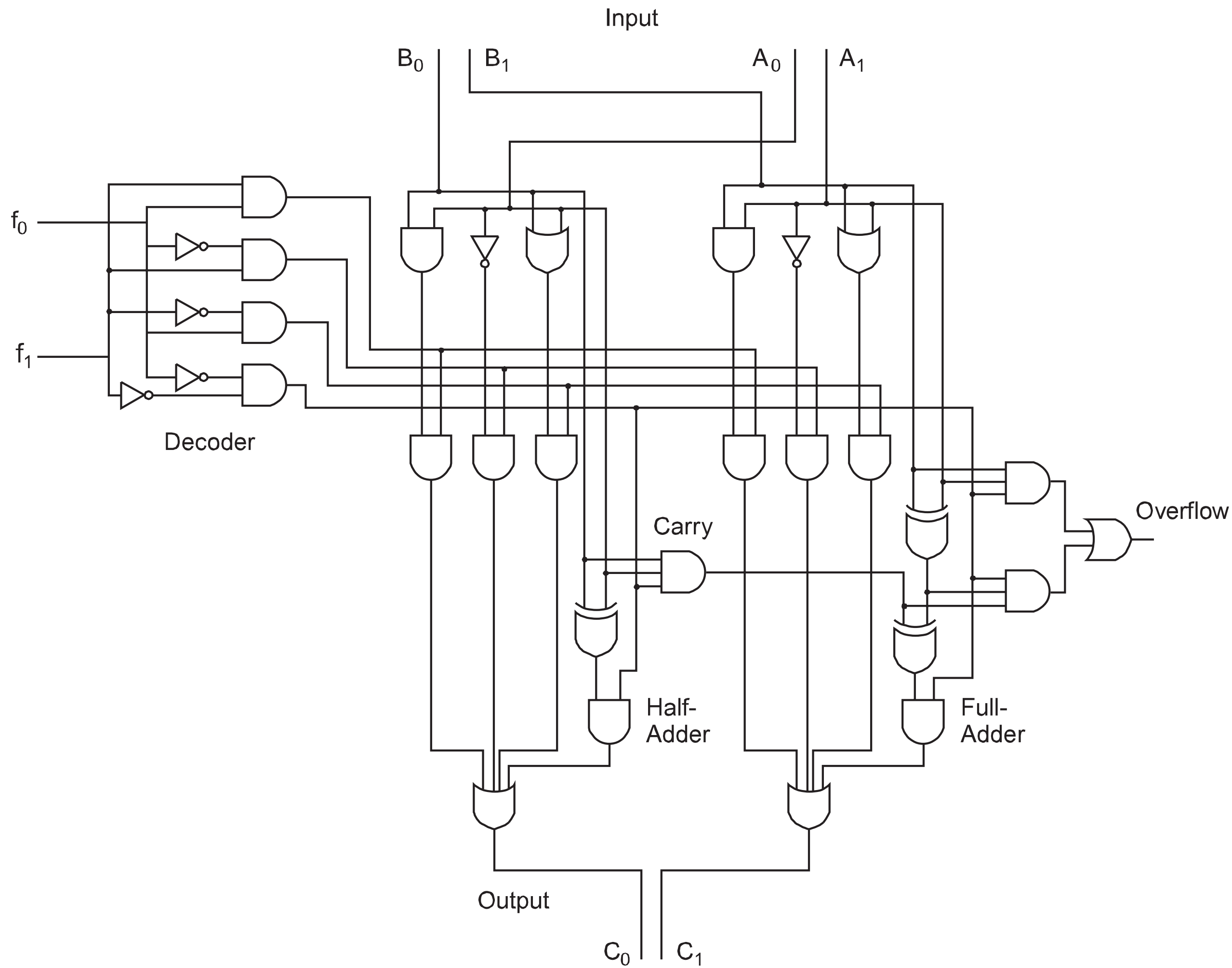
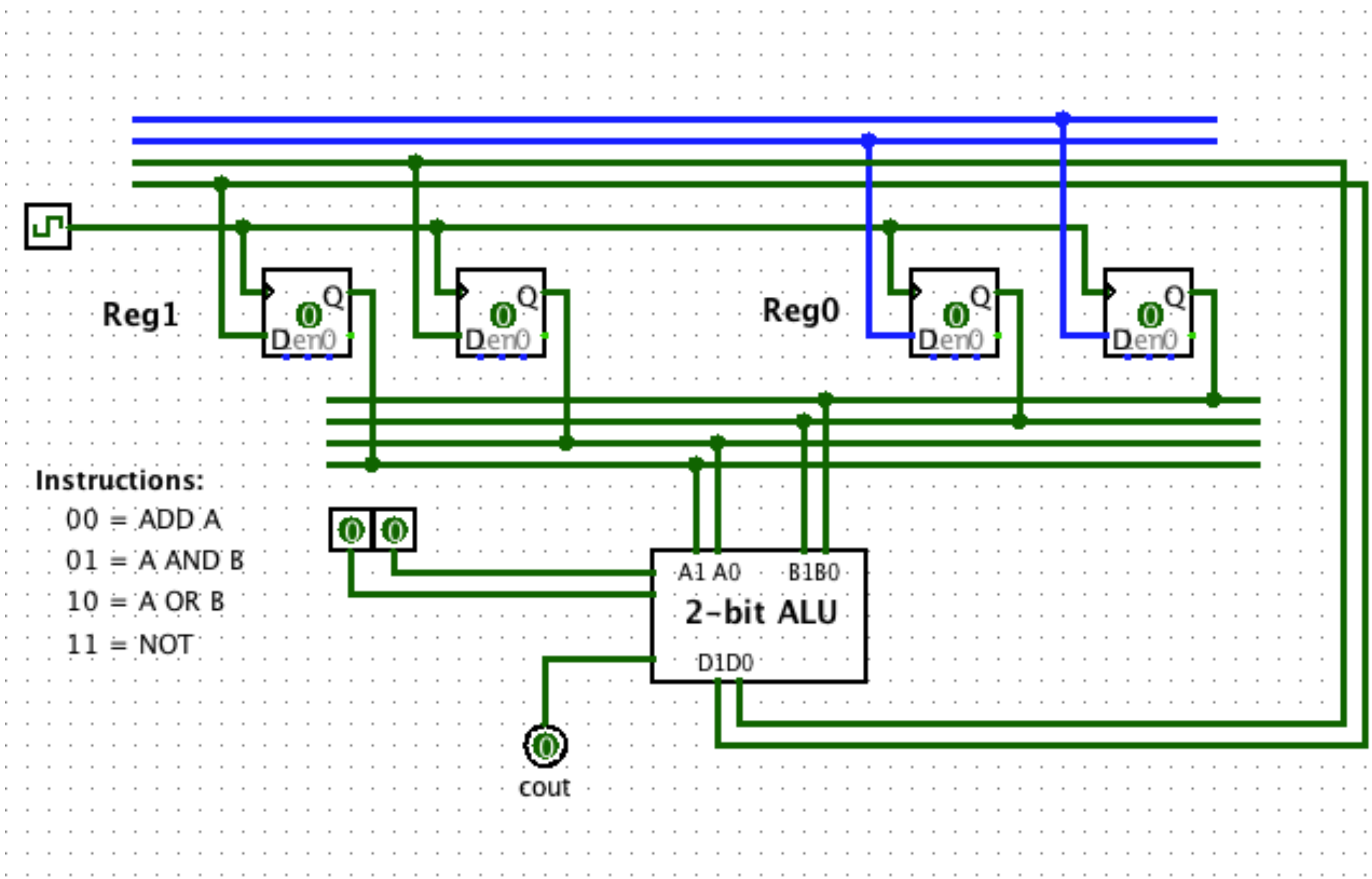


FIGURE 3.17 A Simple Two-Bit ALU



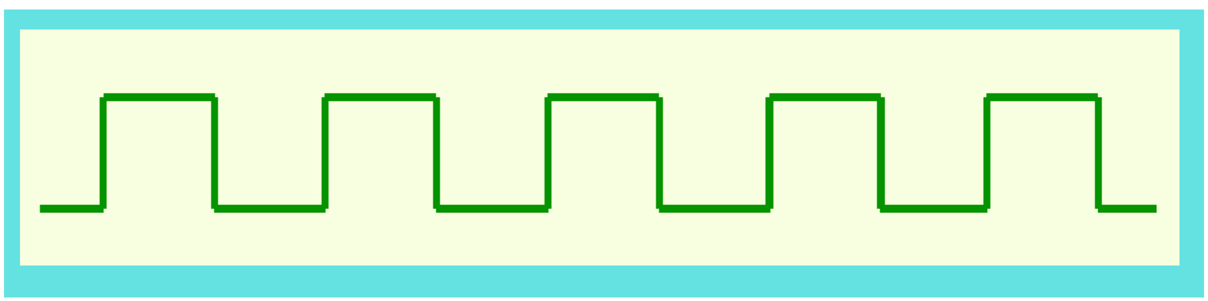
Reg1
Reg0
Instructions:
00 = ADD A
01 = A AND B
10 = A OR B
11 = NOT
A1 A0
B1 B0
2-bit ALU
D1 D0
cout

3.6 Sequential Circuits

- Combinational logic circuits are perfect for situations when we require the immediate application of a Boolean function to a set of inputs.
- There are other times, however, when we need a circuit to change its value with consideration to its current state as well as its inputs.
  - These circuits have to "remember" their current state.
- *Sequential logic circuits* provide this functionality for us.

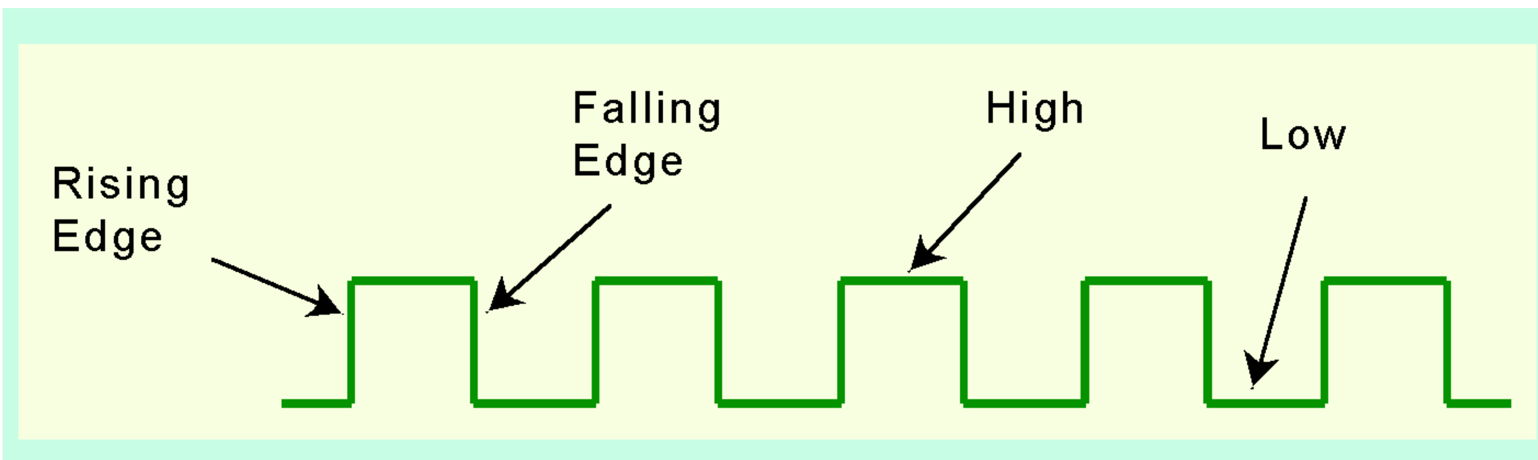
3.6 Sequential Circuits

- As the name implies, sequential logic circuits require a means by which events can be sequenced.
- State changes are controlled by clocks.
  - A "clock" is a special circuit that sends electrical pulses through a circuit.
- Clocks produce electrical waveforms such as the one shown below.



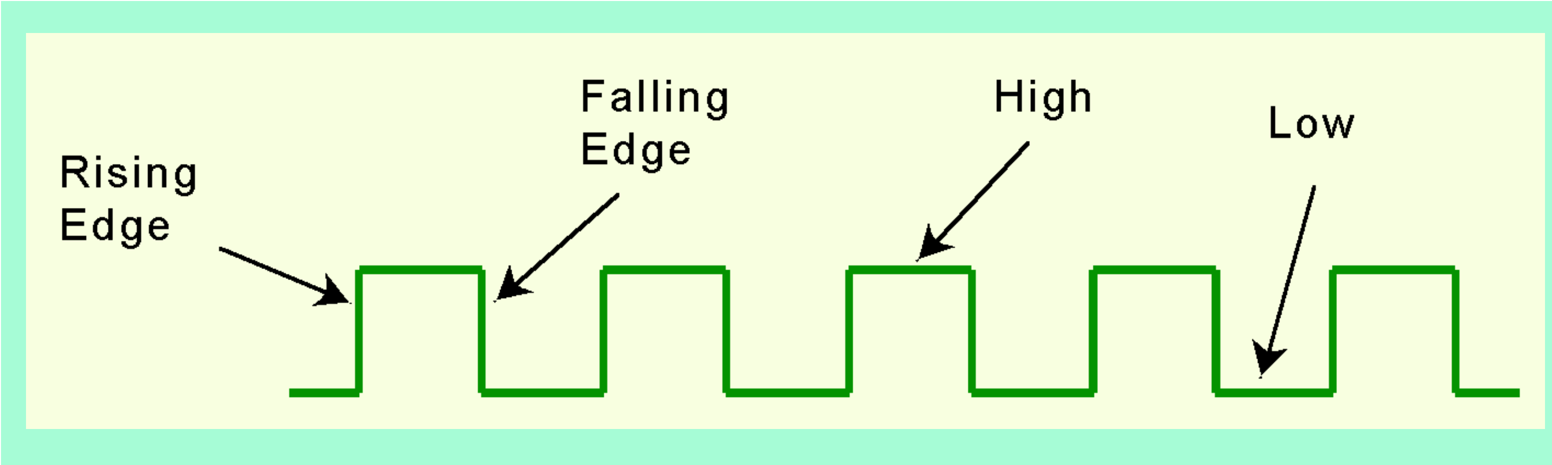
3.6 Sequential Circuits

- State changes occur in sequential circuits only when the clock ticks.
- Circuits can change state on the rising edge, falling edge, or when the clock pulse reaches its highest voltage.



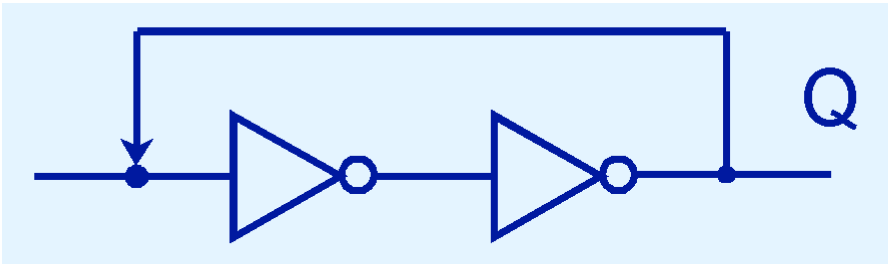
3.6 Sequential Circuits

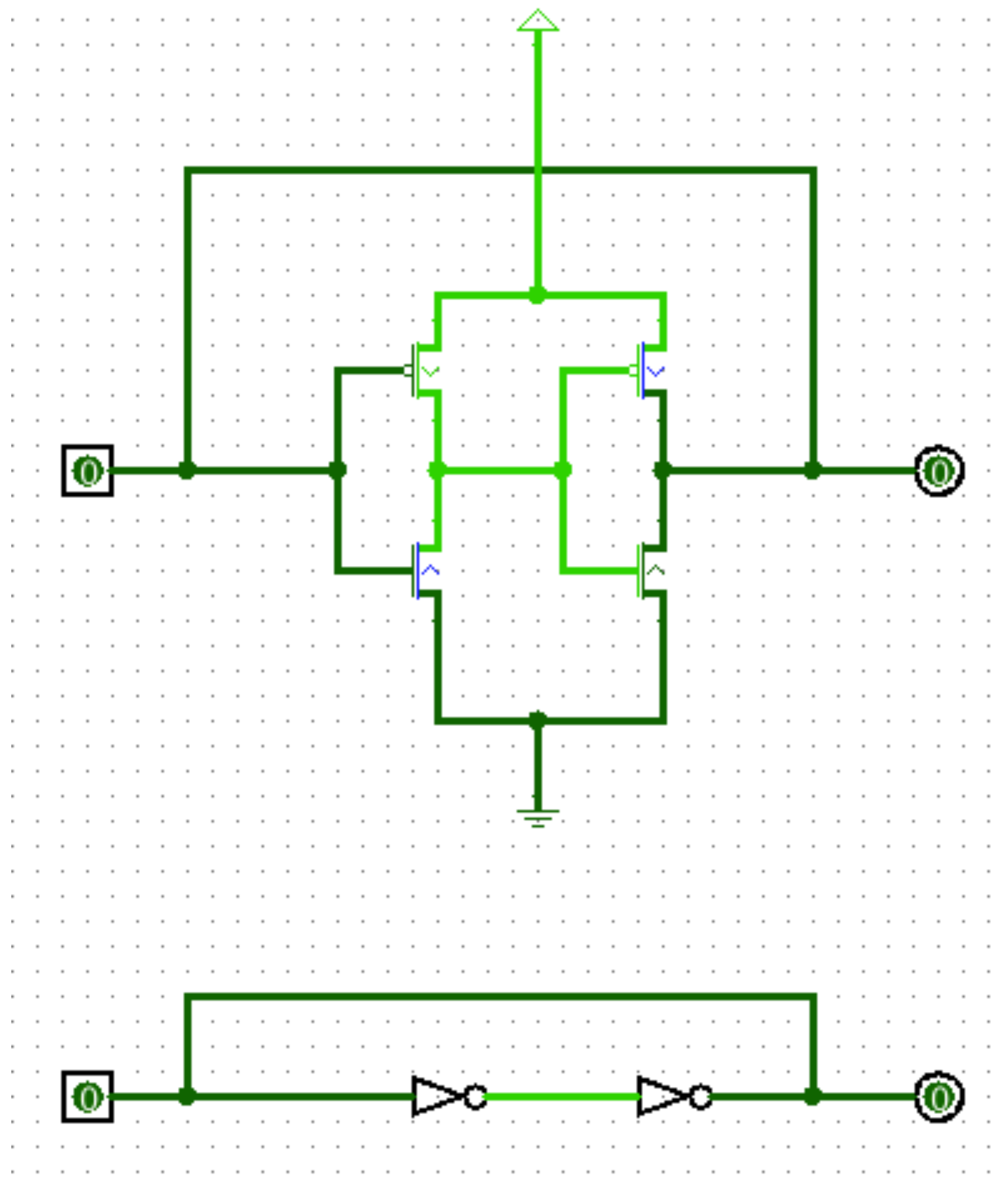
- Circuits that change state on the rising edge, or falling edge of the clock pulse are called *edge-triggered.*
- *Level-triggered circuits* change state when the clock voltage reaches its highest or lowest level.

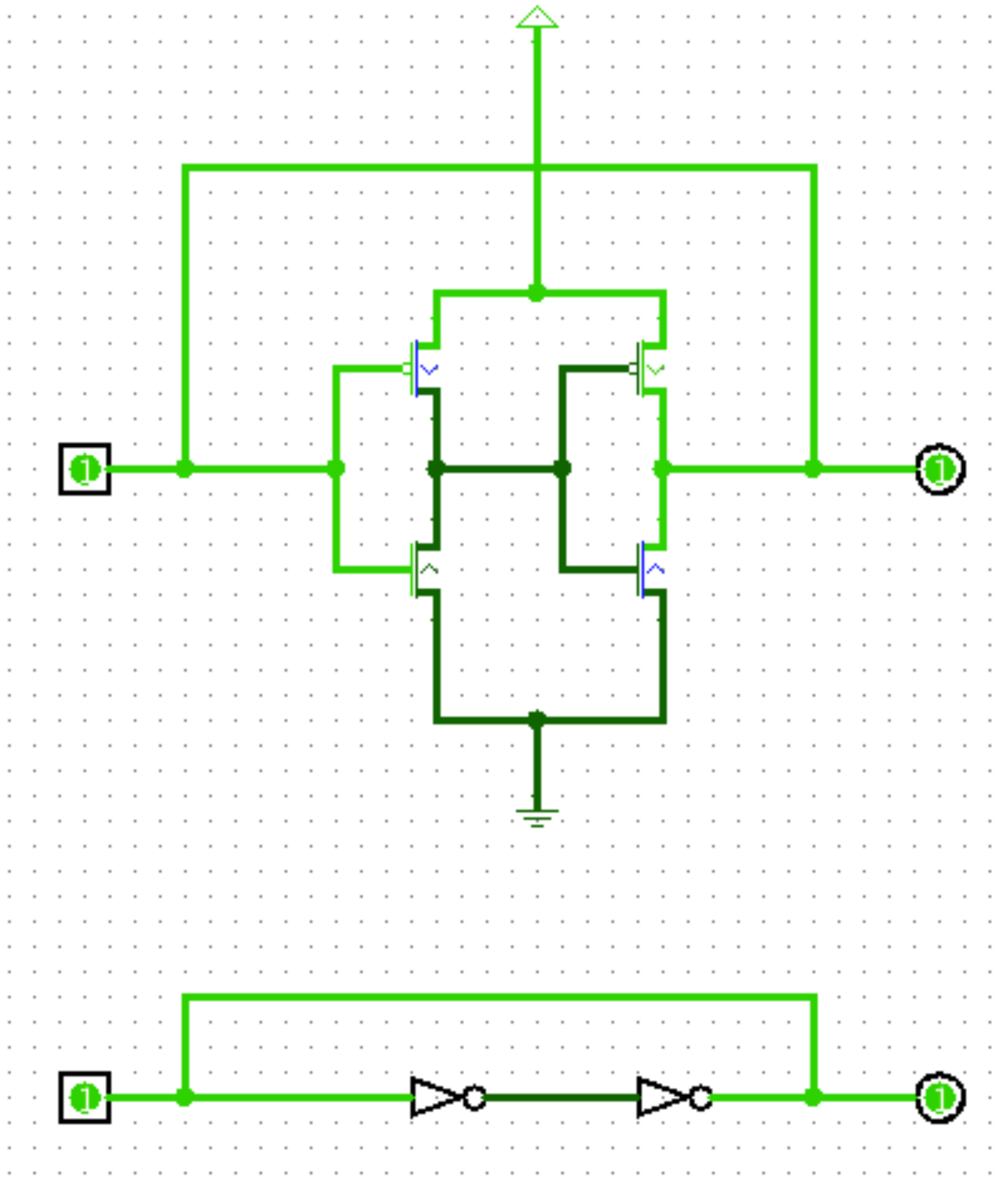


3.6 Sequential Circuits

- To retain their state values, sequential circuits rely on *feedback.*
- Feedback in digital circuits occurs when an output is looped back to the input.
- A simple example of this concept is shown below.
  - If Q is 0 it will always be 0, if it is 1, it will always be 1. Why?



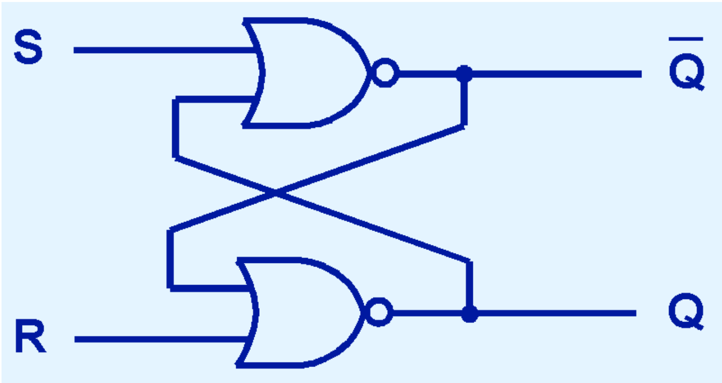

0
0
0
0

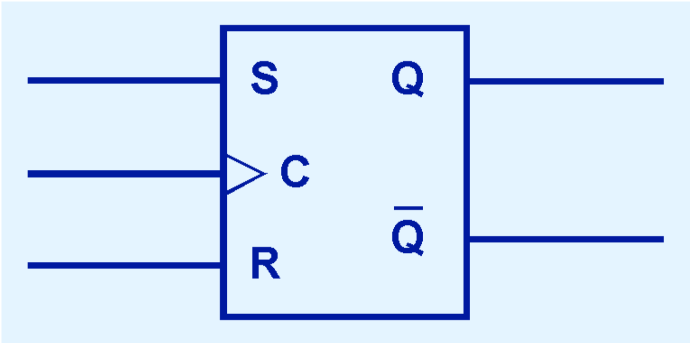


FLIP-FLOPS

3.6 Sequential Circuits

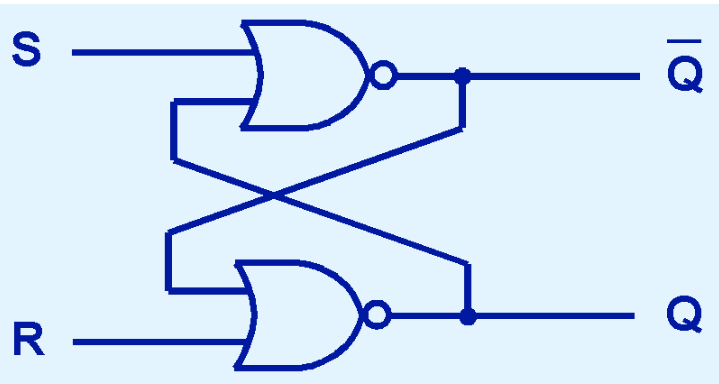
- You can see how feedback works by examining the most basic sequential logic components, the SR flip-flop.
  - The "SR" stands for set/reset.
- The internals of an SR flip-flop are shown below, along with its block diagram.





3.6 Sequential Circuits

- The behavior of an SR flip-flop is described by a characteristic table.
- Q(t) means the value of the output at time t. Q(t+1) is the value of Q after the next clock pulse.



S	R	Q(t+1)
0	0	Q(t) (no change)
0	1	0 (reset to 0)
1	0	1 (set to 1)
1	1	undefined

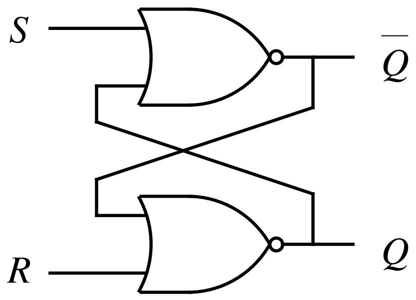
3.6 Sequential Circuits

- The SR flip-flop actually has three inputs: S, R, and its current output, Q.
- Thus, we can construct a truth table for this circuit, as shown at the right.
- Notice the two undefined values. When both S and R are 1, the SR flip-flop is unstable.

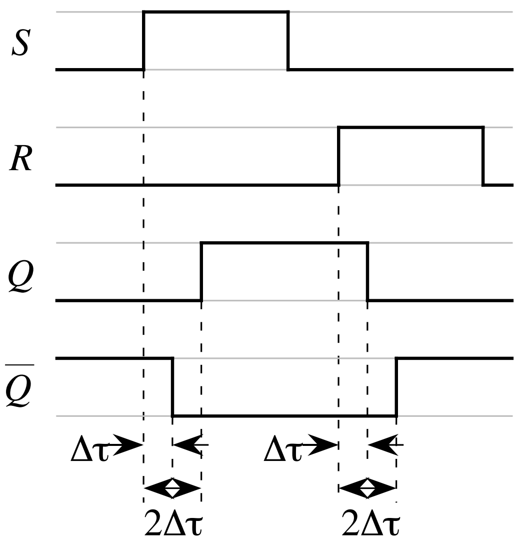
S	R	Present State Q(t)	Next State Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	undefined
1	1	1	undefined

S-R Flip-Flop

- The S-R flip-flop is an active high (positive logic) device.

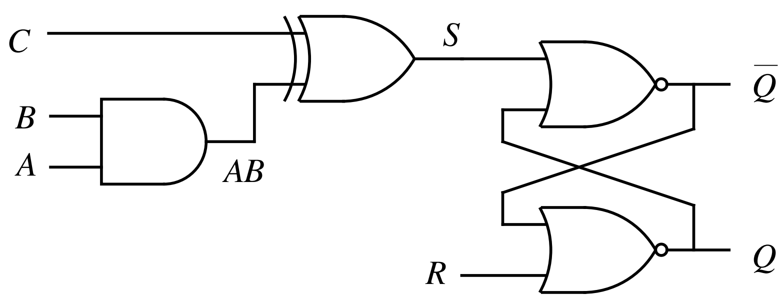


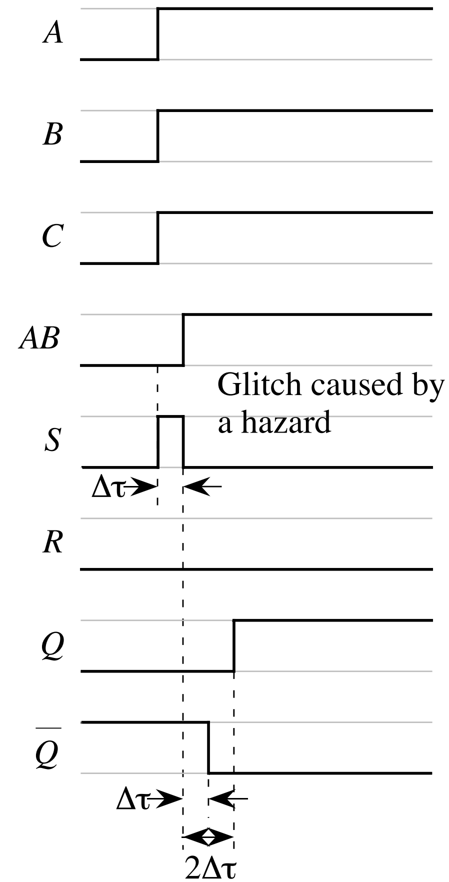
Q_t	S_t	R_t	Q_{i+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	(disallowed)
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	(disallowed)



Timing Behavior

A Hazard

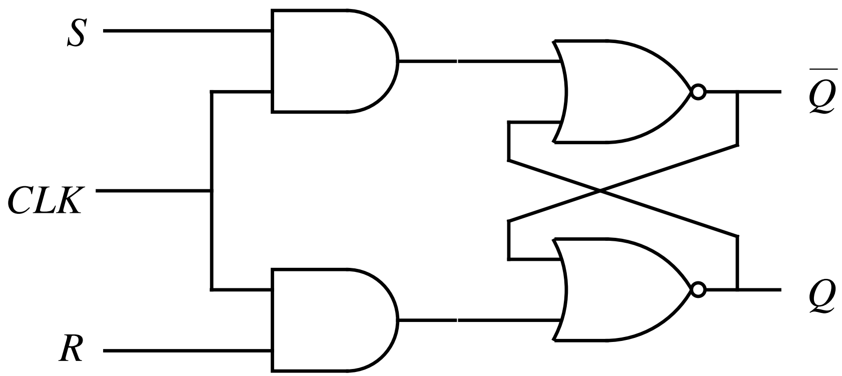


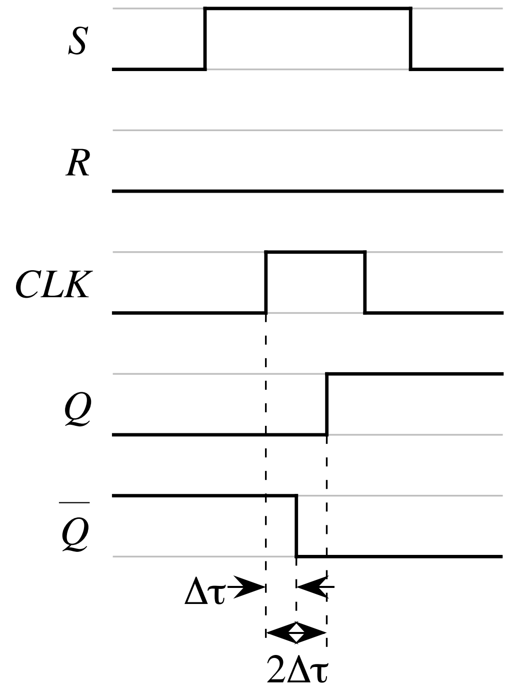


Timing Behavior

- **It is desirable to be able to "turn off" the flip-flop so it does not respond to such hazards.**

Clocked S-R Flip-Flop



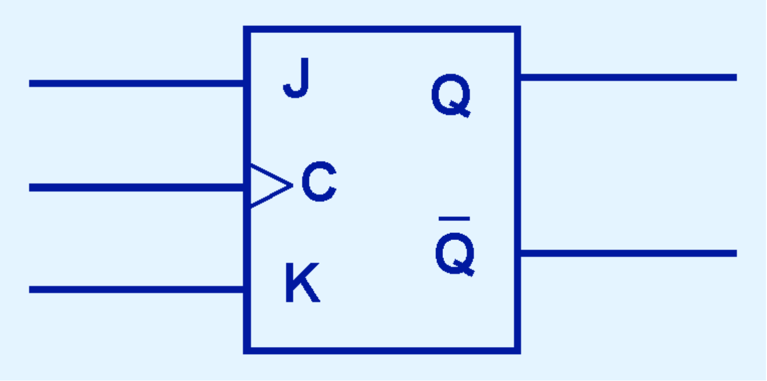


Timing Behavior

- **The clock signal, CLK, enables the S and R inputs to the flip-flop.**

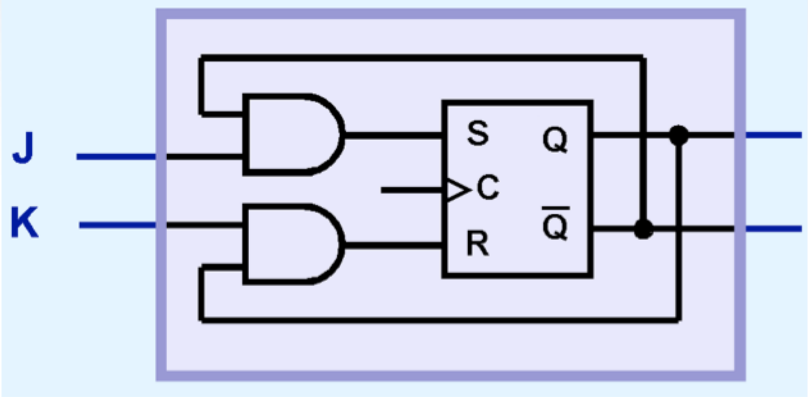
3.6 Sequential Circuits

- If we can be sure that the inputs to an SR flip-flop will never both be 1, we will never have an unstable circuit. This may not always be the case.
- The SR flip-flop can be modified to provide a stable state when both inputs are 1.
- This modified flip-flop is called a JK flip-flop, shown at the right.
  - The "JK" is in honor of Jack Kilby.



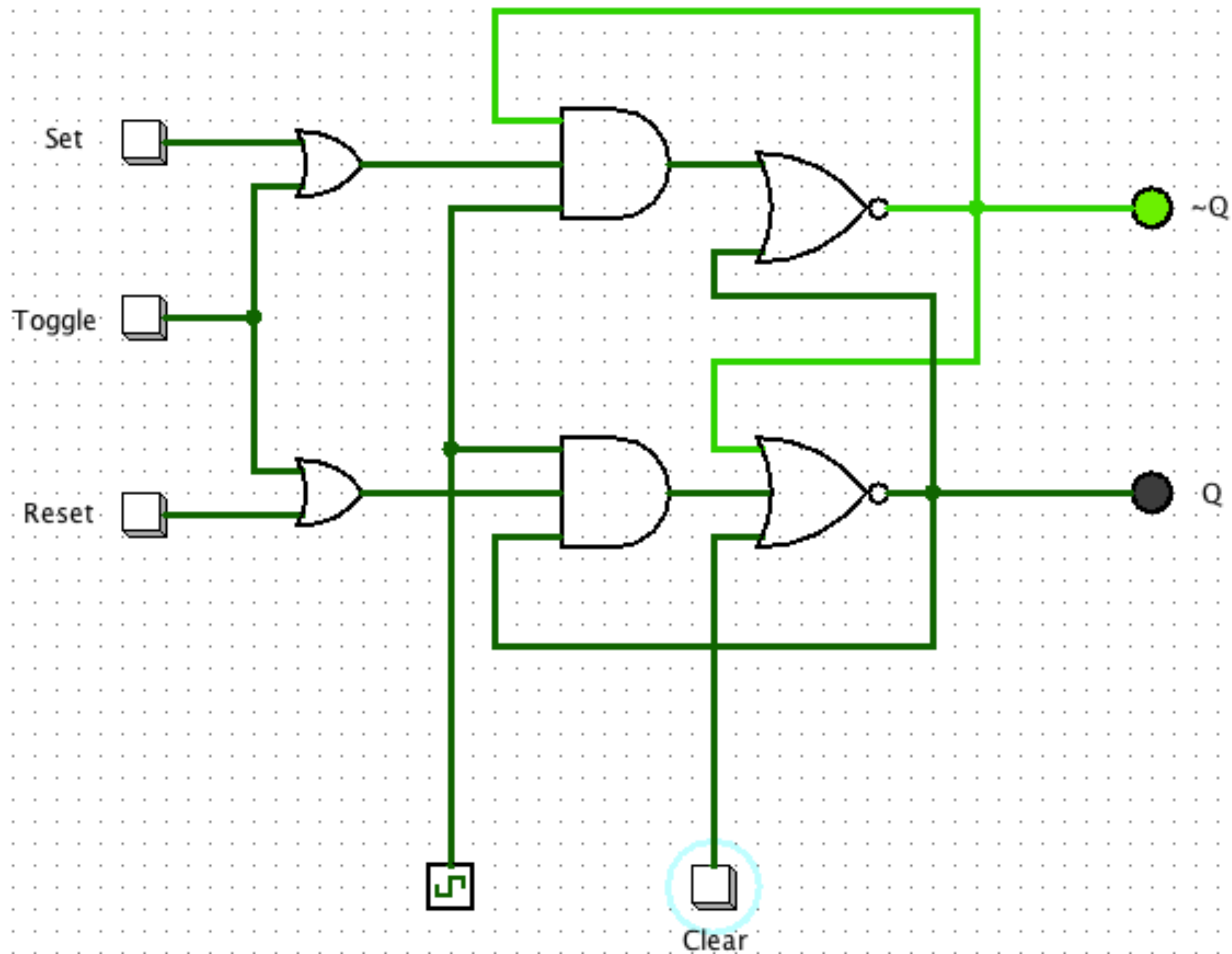
3.6 Sequential Circuits

- At the right, we see how an SR flip-flop can be modified to create a JK flip-flop.
- The characteristic table indicates that the flip-flop is stable for all inputs.



J	K	Q(t+1)
0	0	Q(t) (no change)
0	1	0 (reset to 0)
1	0	1 (set to 1)
1	1	$\overline{Q}$(t)

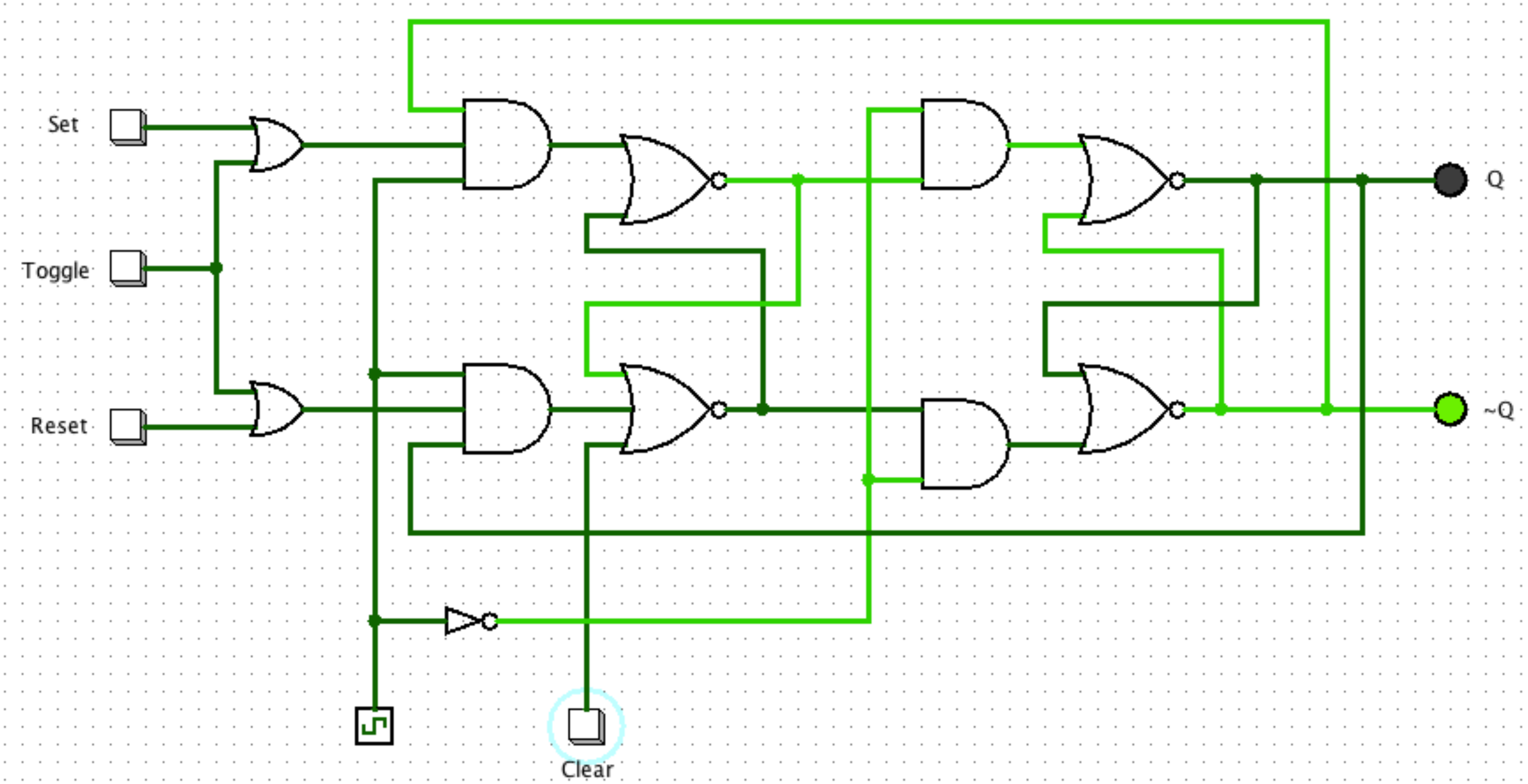
J-K Flip Flop



LATCHES VS FLIP-FLOPS

- **Latch**
  - Output changes right after the input changes
  - No reference to clocking event
  - An “SR flip-flop” is often called an SR latch in other texts.
- **Level-Sensitive Latch**
  - A latch that operates only when the clock is high or only when low
  - The “clocked SR flip-flop” is a level sensitive latch
- **Flip-Flop**
  - Reserved for circuits that record the input only during clocking events
  - The output of the flip-flop does not change during this clocking event
  - A “master-slave flip-flop” fits this definition

Master-Slave J-K Flip Flop

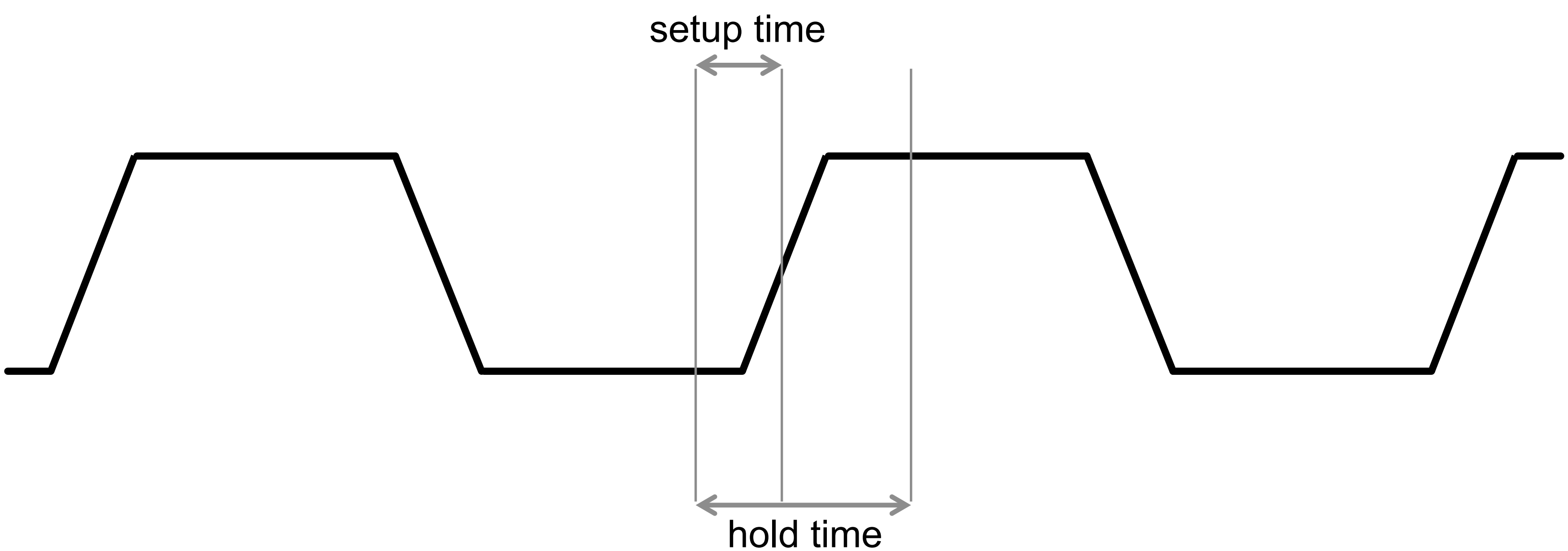


J-K FLIP FLOPS

- Allows both "set" and "reset" to be 1
- When both J and K are 1, the output *toggles*
- If the clock is high, *endless toggle* occurs
- Master-Slave J-K flip-flops solve the endless toggle problem, but have the *ones-catching* problem.
- Edge-triggered flip-flops eliminate the ones-catching problem.

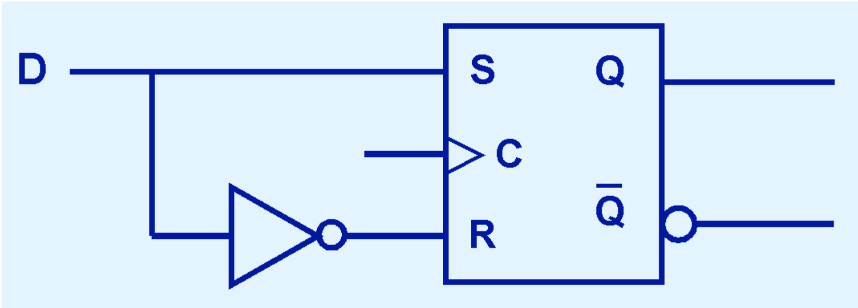
EDGE-TRIGGERED FLIP-FLOPS

- **Records input during a low-to-high (positive edge) or a high-to-low (negative edge) clock transition**
- **Signal must be stable before *setup time* and continue to be stable for *hold time***



3.6 Sequential Circuits

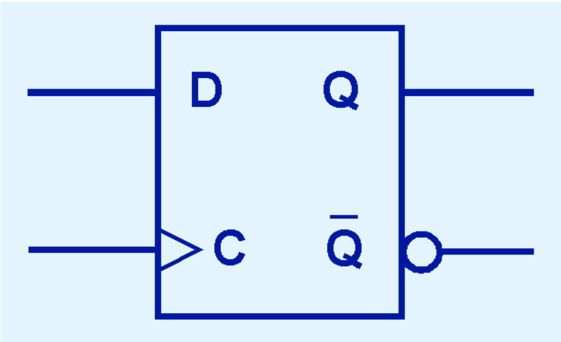
- Another modification of the SR flip-flop is the D flip-flop, shown below with its characteristic table.
- You will notice that the output of the flip-flop remains the same during subsequent clock pulses. The output changes only when the value of D changes.



D	Q(t+1)
0	0
1	1

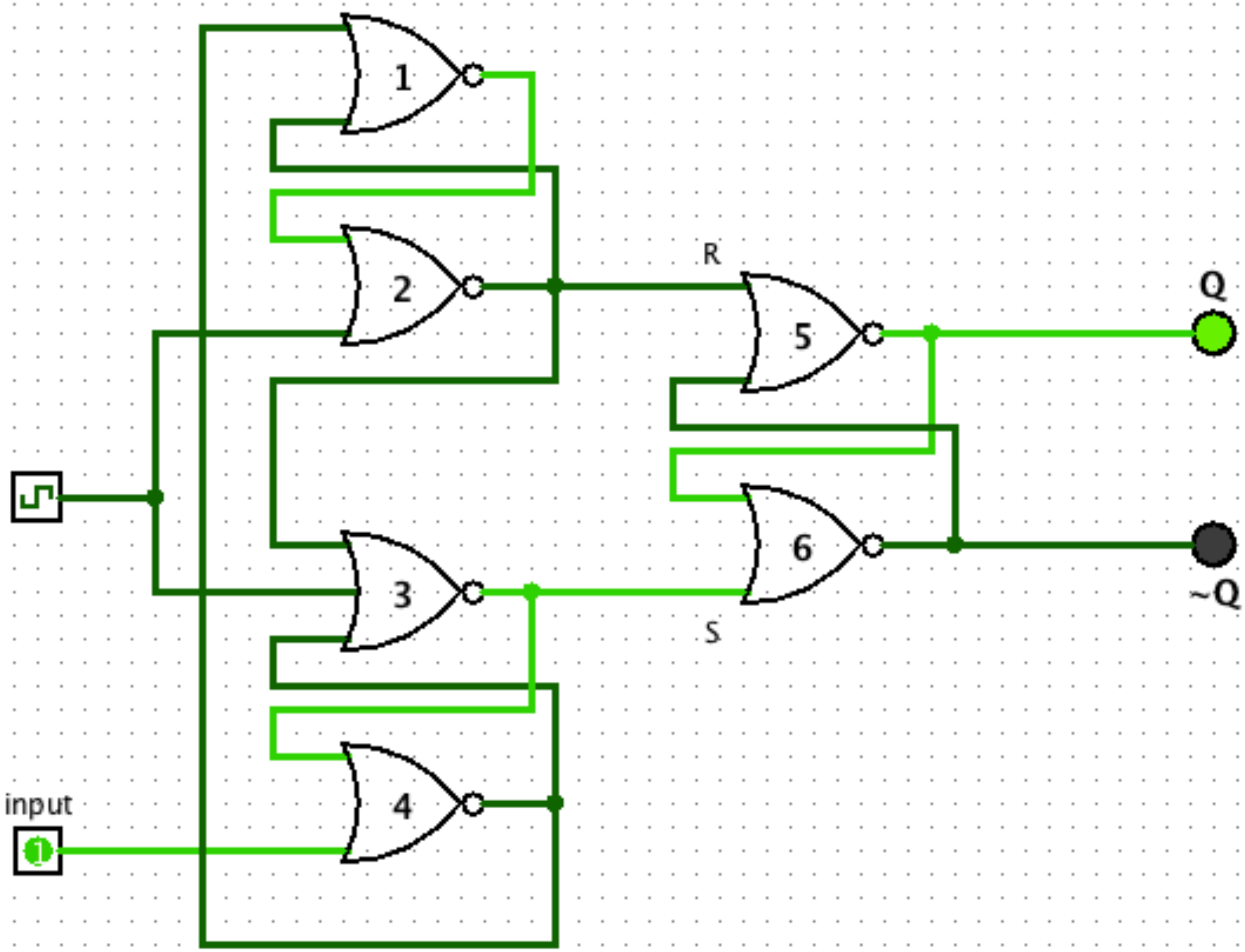
3.6 Sequential Circuits

- The D flip-flop is the fundamental circuit of computer memory.
  - D flip-flops are usually illustrated using the block diagram shown below.
- The characteristic table for the D flip-flop is shown at the right.



D	Q(t+1)
0	0
1	1

Negative Edge-Triggered D Flip-Flop



Explanation of function of negative edge-triggered D flip-flop:

1. All gates are NOR gates, which has the following truth-table:

X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

2. Gates 5 & 6 form an SR latch. When inputs to SR latch are both low, nothing happens --- the latched value remains.

3. We need the invariant that when the clock is low then the outputs of Gate 2 and Gate 3 are opposite values.

4. When the clock is low, changing the input does not change the outputs of Gates 2 & 3. Therefore, changing the input will not change the value latched by Gates 5 & 6. Here's why:

   a. If the output of Gate 2 is 1, this forces the output of Gate 1 to be 0 and also forces the output of Gate 3 to be zero. Therefore, changing the input cannot change the outputs of Gates 2 & 3. Furthermore, both inputs to Gate 2 are 0, which maintains the output of Gate 2 at 1.
   b. If the output of Gate 2 is 0, then by our invariant, the output of Gate 3 must be 1. This forces the output of Gate 4 to be 0. Therefore, changing the input does not affect the output of Gate 4 and so cannot change anything else in the circuit. In particular, all of the inputs to Gate 3 remain at 0 and the output of Gate 3 stays at 1.

5. When the clock is high, the outputs of Gates 2 & 3 are always 0, regardless of the input. So, the value latched by Gates 5 & 6 cannot change when the clock is high.

6. When the clock is high, the outputs of Gates 1 & 4 are controlled by the input. However, we still know that the value of Gates 1 & 4 will be opposite. In particular, the output of Gate 1 is equal to the input value and the output of Gate 4 is the opposite of the input value.

7. Note, when the gate is high, input is *not* latched by Gates 1 & 4. I.e., changing the input continues to alter Gates 1 & 4 as long as the clock remains high. This shows that the flip-flop does *not* have the ones-catching problem.

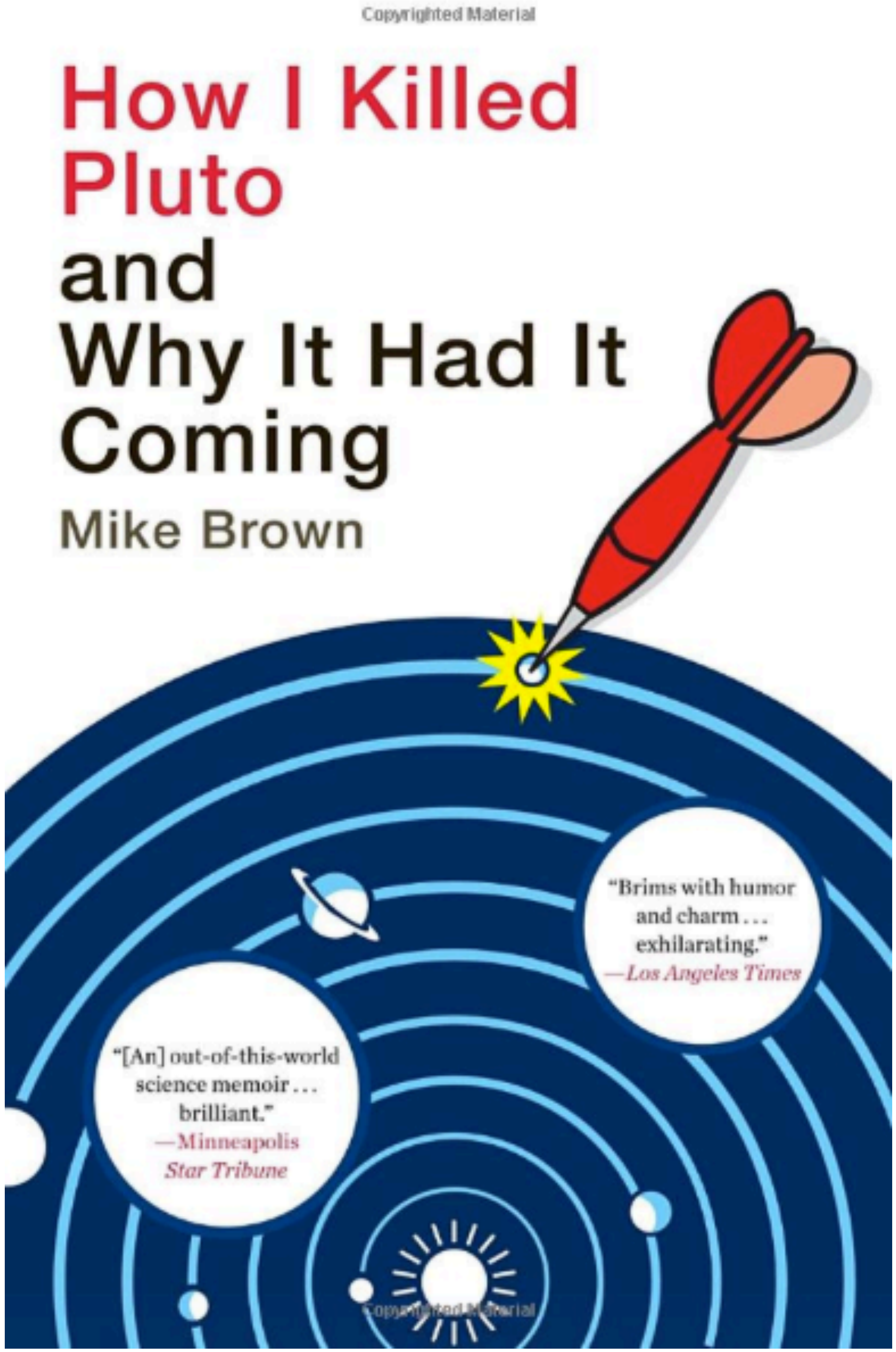
8. Before the setup time, the input must be stable. So, the outputs of Gate 1 and Gate 4 will also settle on some value.

9. When the clock goes from high to low, Gates 2 and 3 act like inverters for the outputs of Gates 1 and 4. The output of Gates 2 and 3 are thus guaranteed to be opposite (which maintains our invariant). These opposite values are then latched by Gates 5 and 6.

MASTER-SLAVE VS EDGE-TRIGGERED

- **Master-slave flip-flops record the input in the slave when the clock goes from high to low.**
- **Are master-slave flip-flops negative edge-triggered flip-flops?**
  - Some textbooks say "yes" others say "no"
  - Master-slave J-K flip-flops have the ones-catching problem (momentary high signal at J when the clock is high is *caught* and recorded).
  - Master-slave D flip-flops do not have the ones-catching problem.

- **Is Pluto a planet??**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