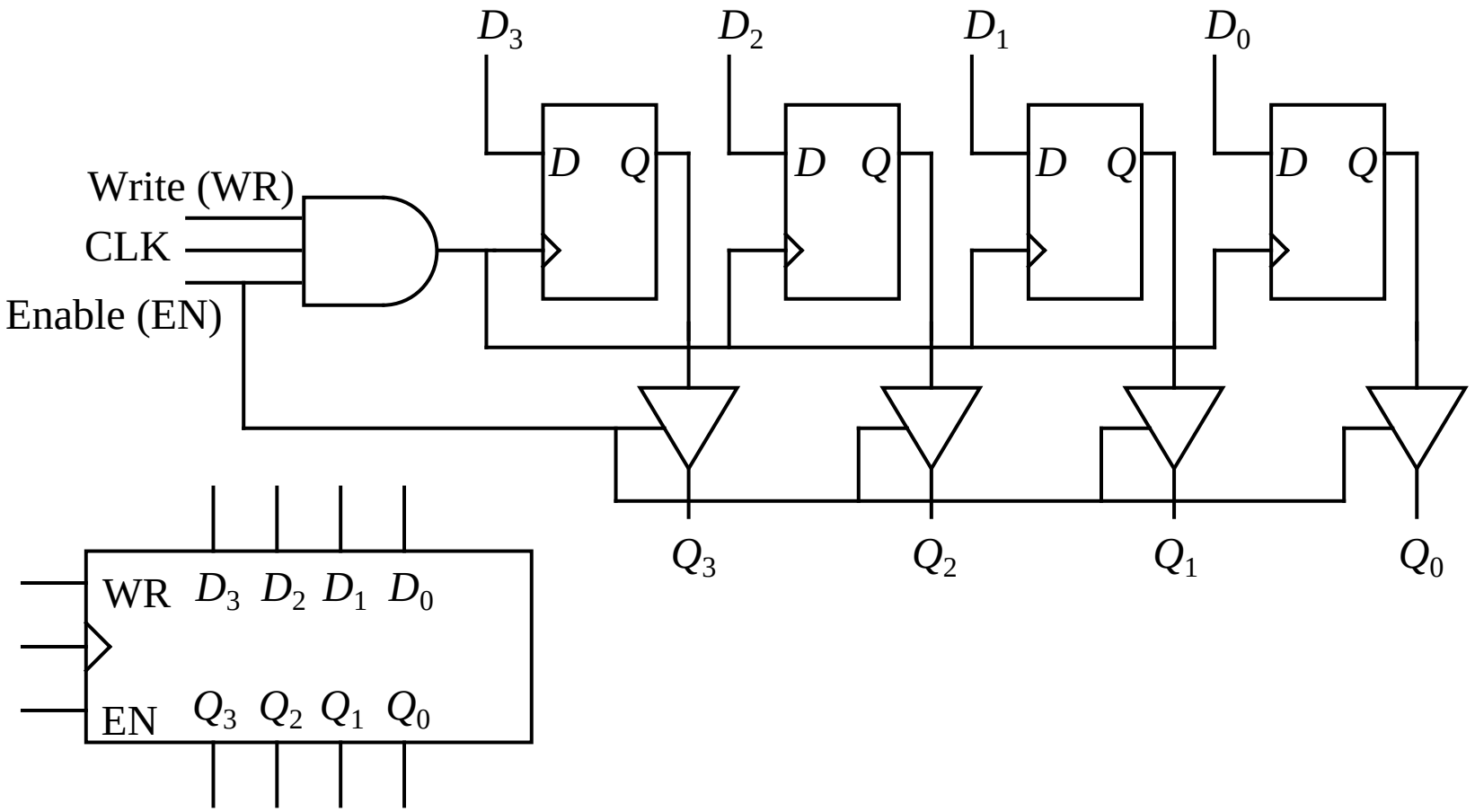
CMSC 313 Lecture 25

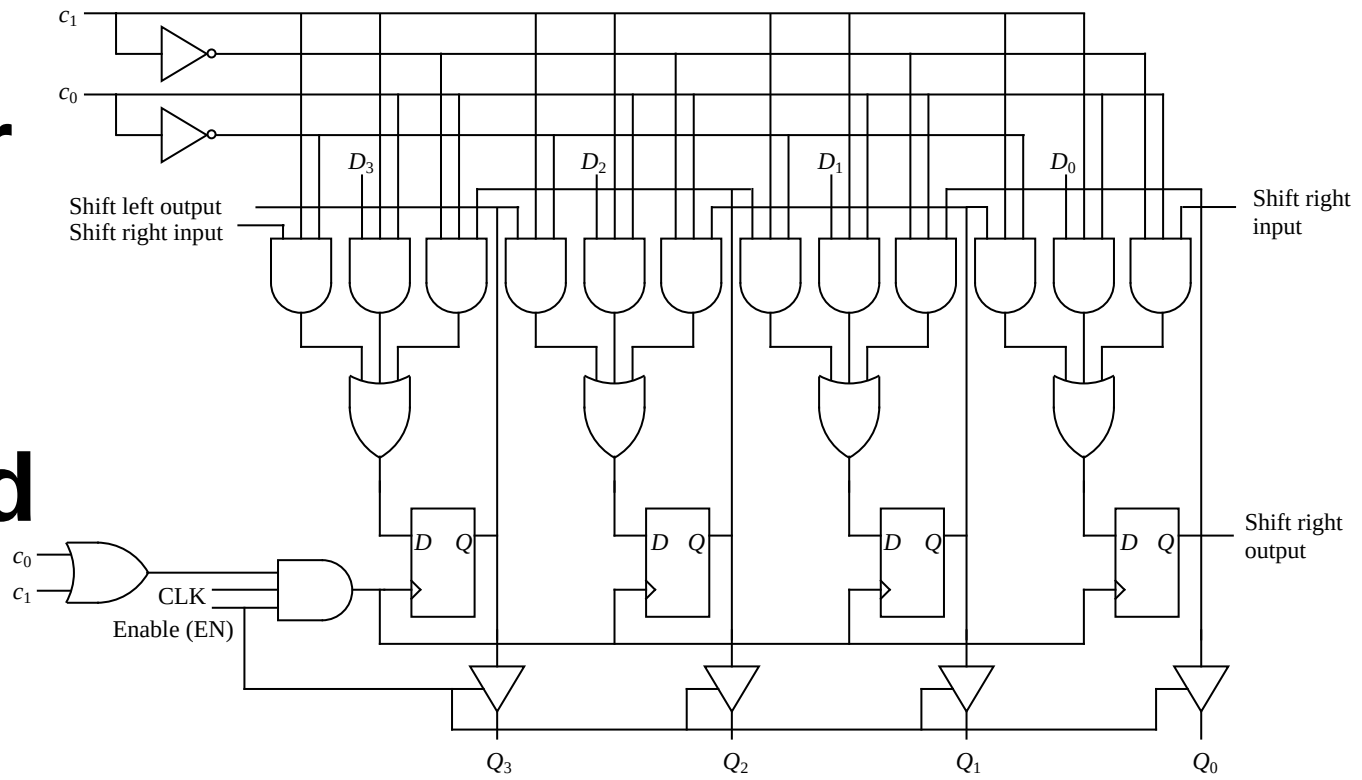
- Registers
- Memory Organization
- DRAM

Four-Bit Register

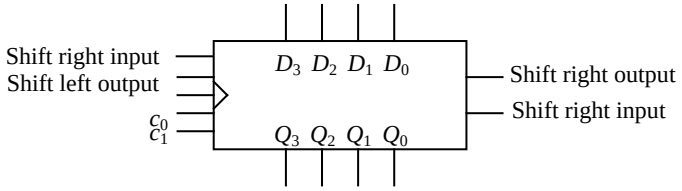
- **Makes use of tri-state buffers so that multiple registers can gang their outputs to common output lines.**



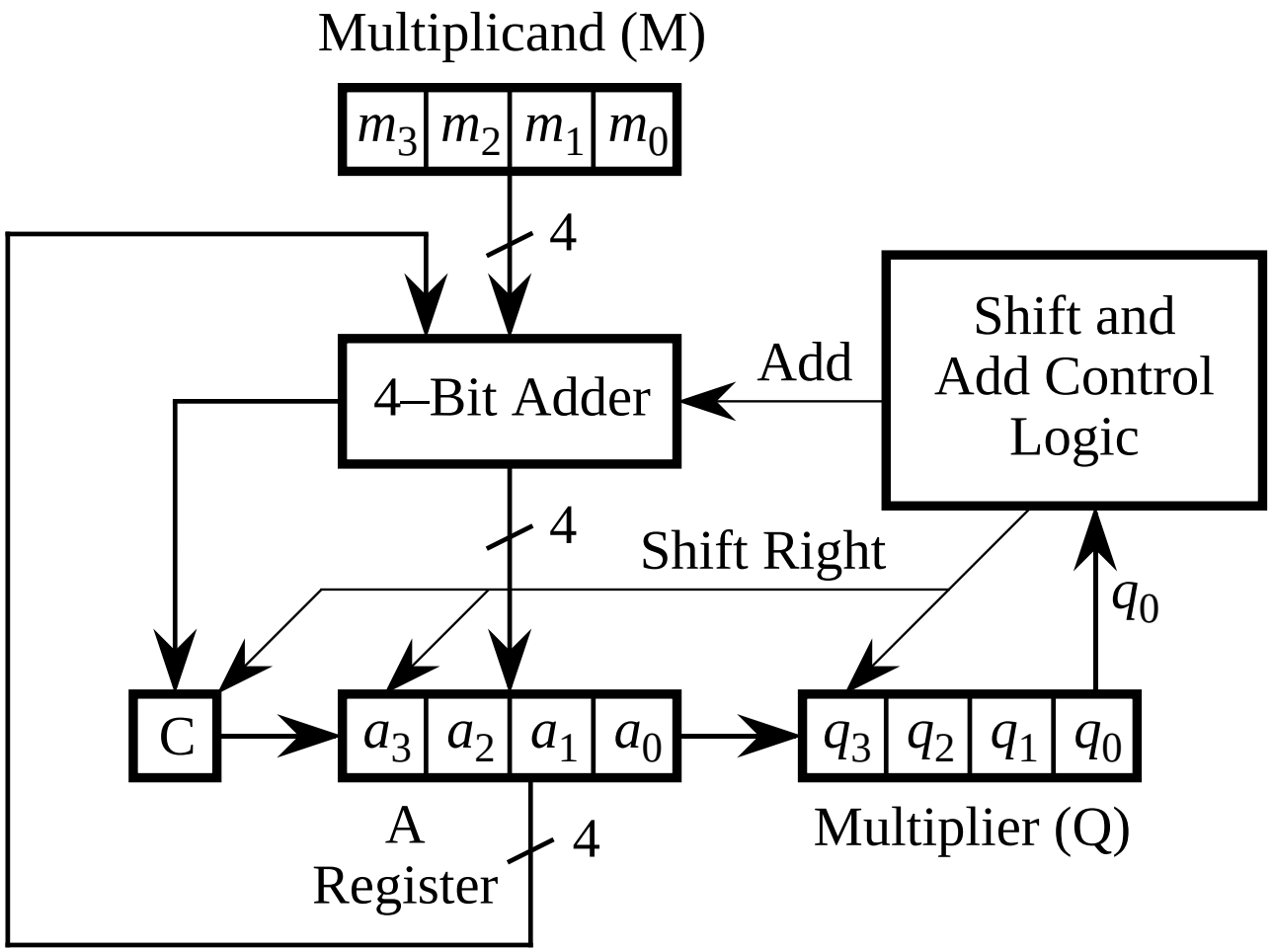
Left-Right Shift Register with Parallel Read and Write



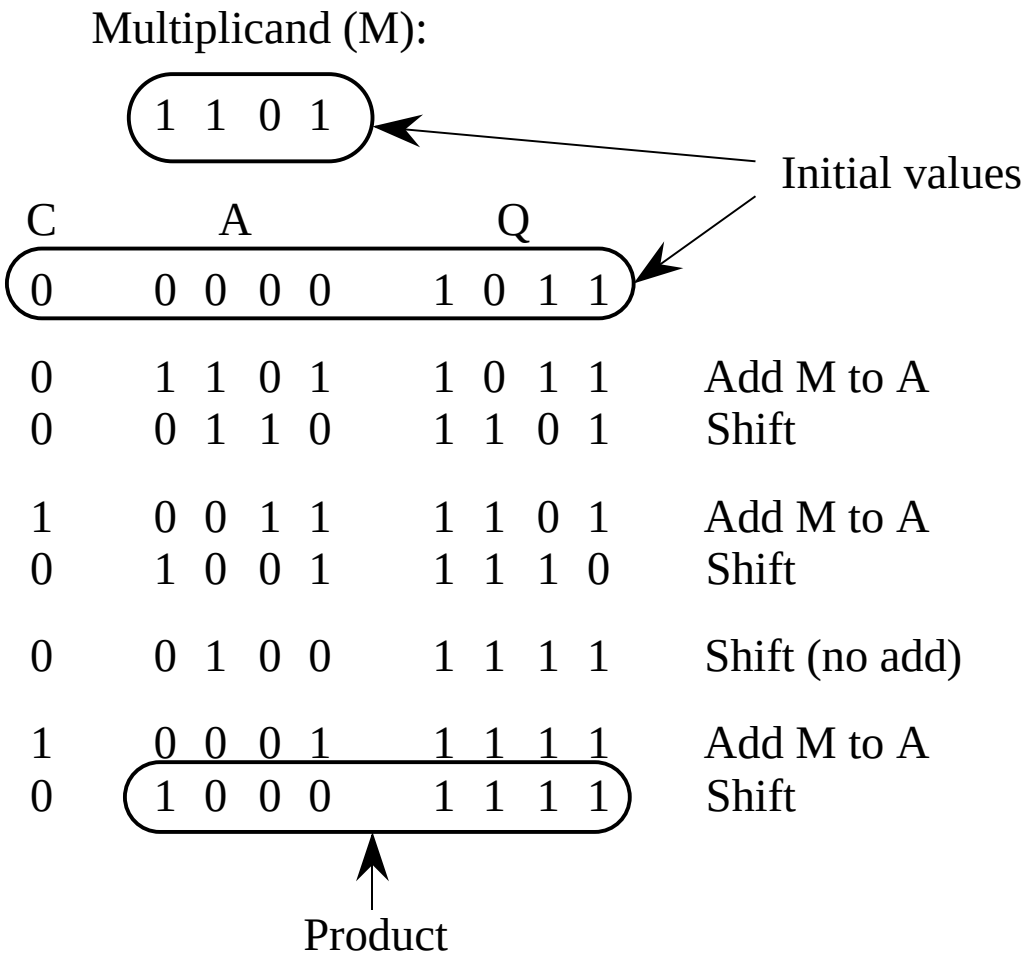
Control c_1	Control c_0	Function
0	0	No change
0	1	Shift left
1	0	Shift right
1	1	Parallel load



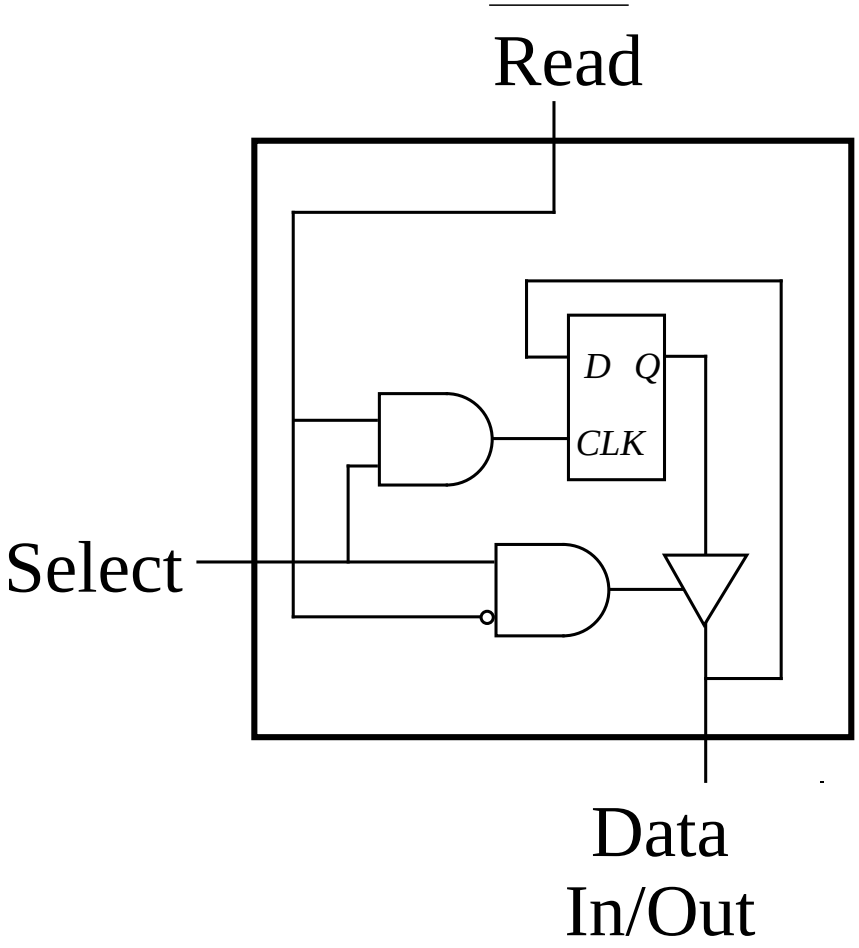
A Serial Multiplier



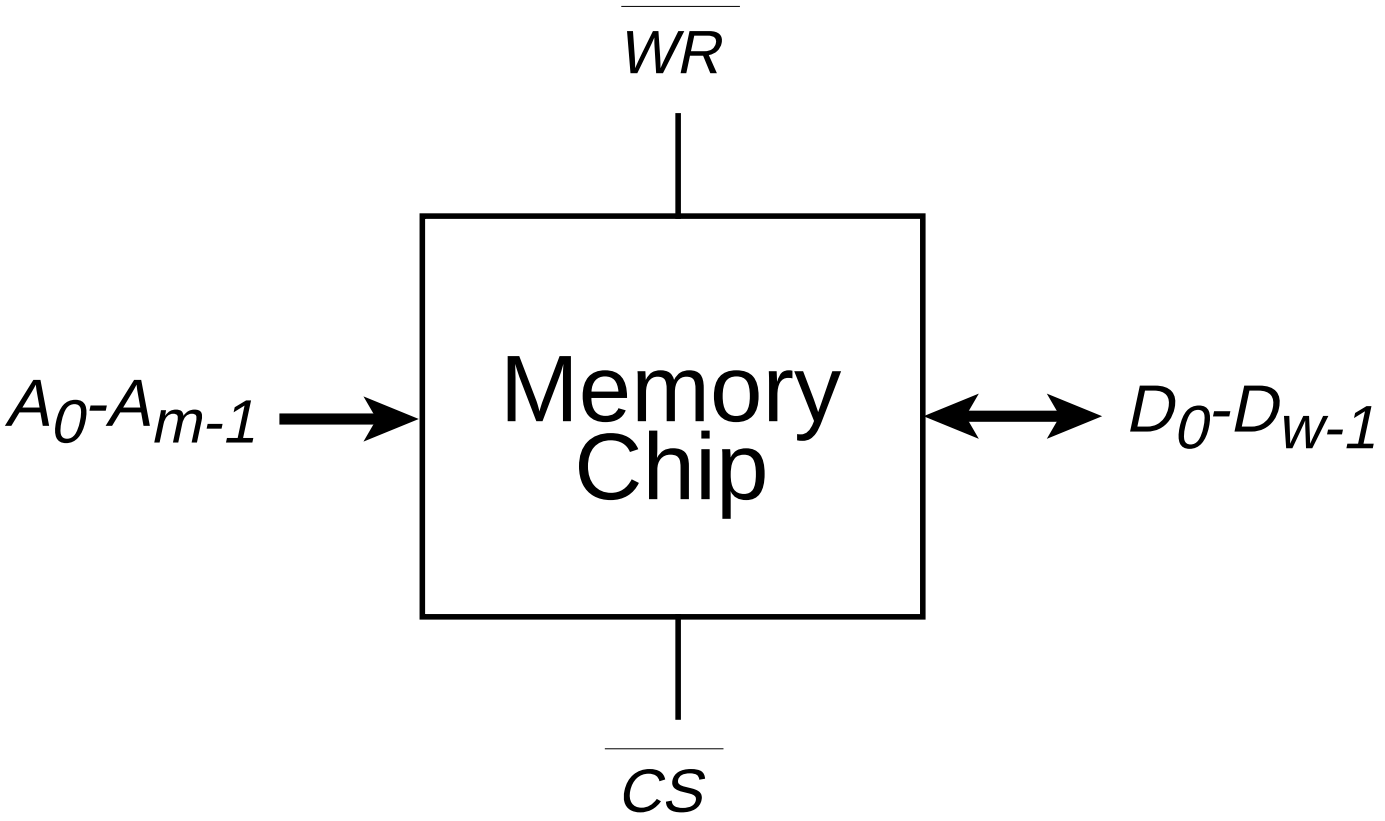
Example of Multiplication Using Serial Multiplier



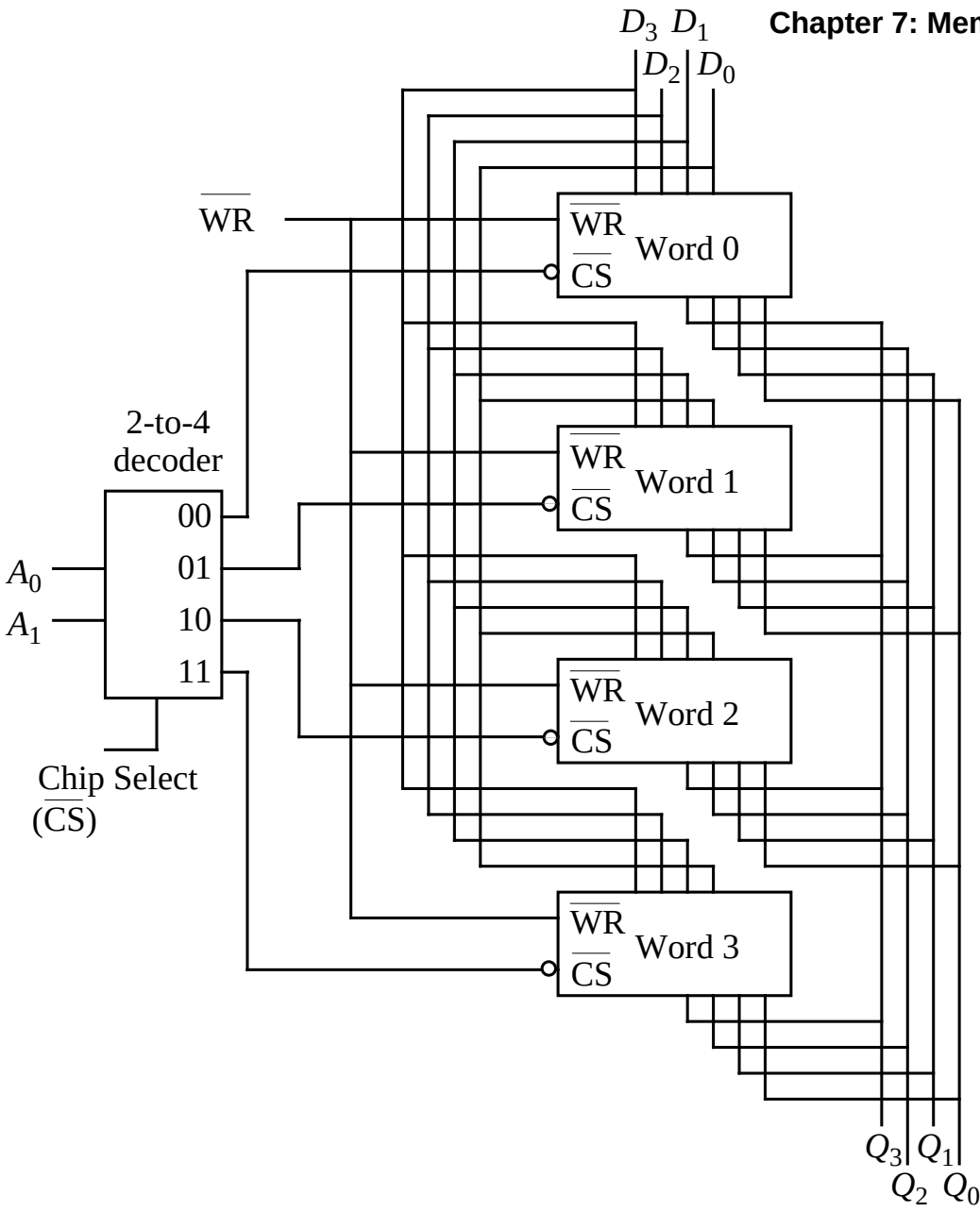
Functional Behavior of a RAM Cell



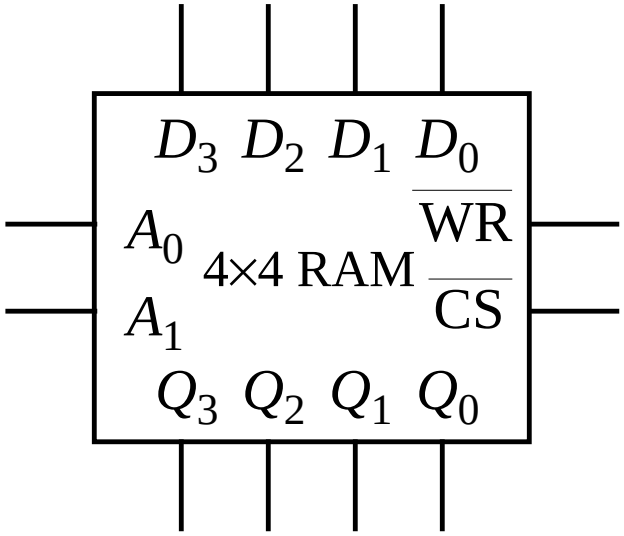
Simplified RAM Chip Pinout



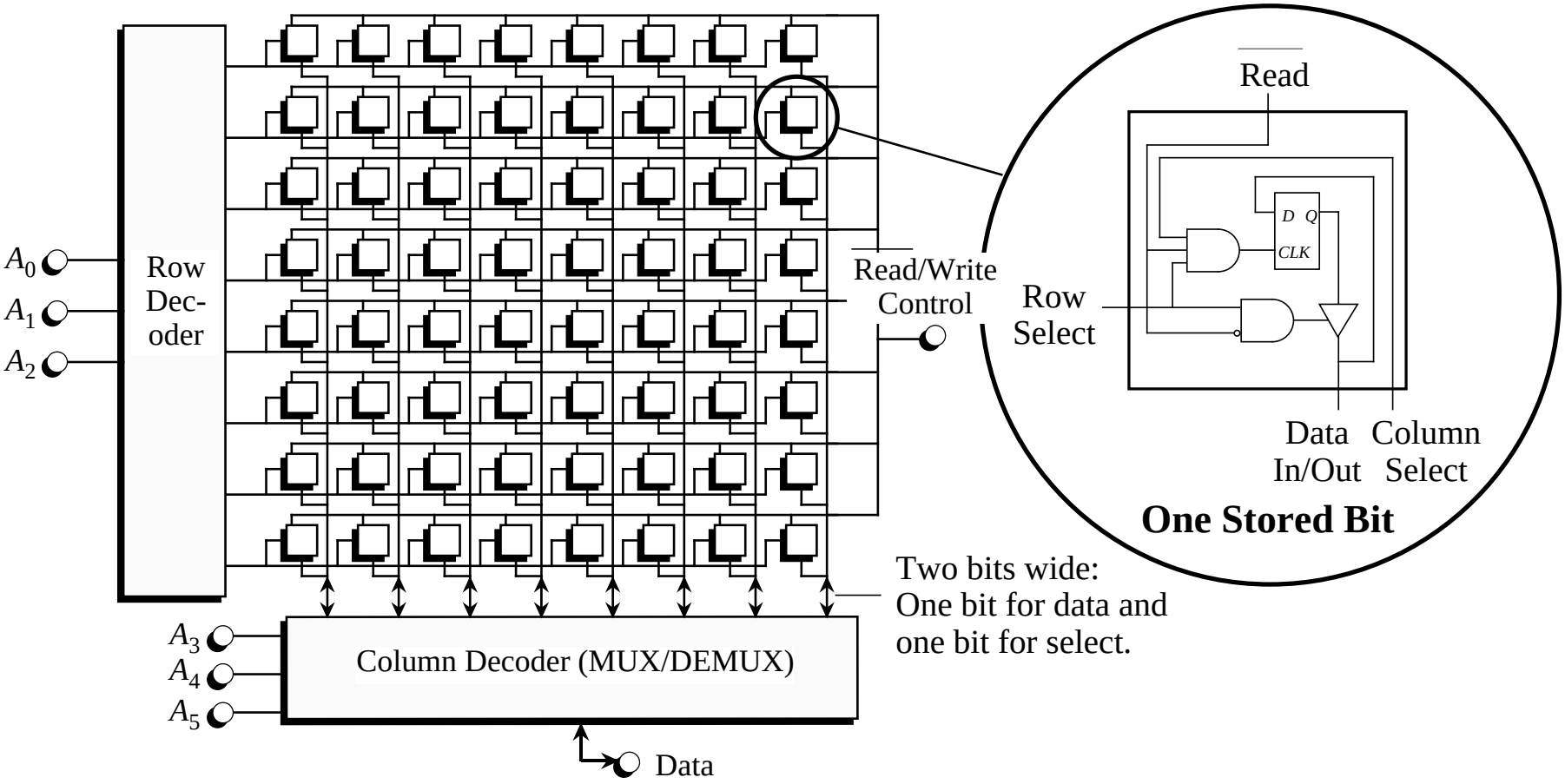
A Four-Word Memory with Four Bits per Word in a 2D Organization



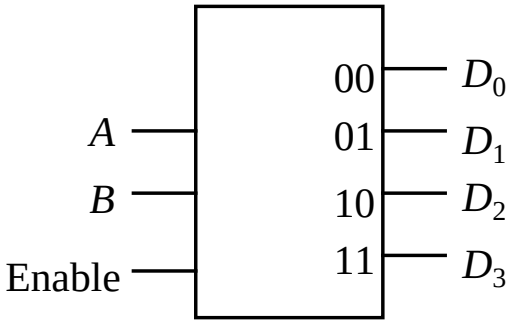
A Simplified Representation of the Four-Word by Four-Bit RAM



2-1/2D Organization of a 64-Word by One-Bit RAM



Decoder

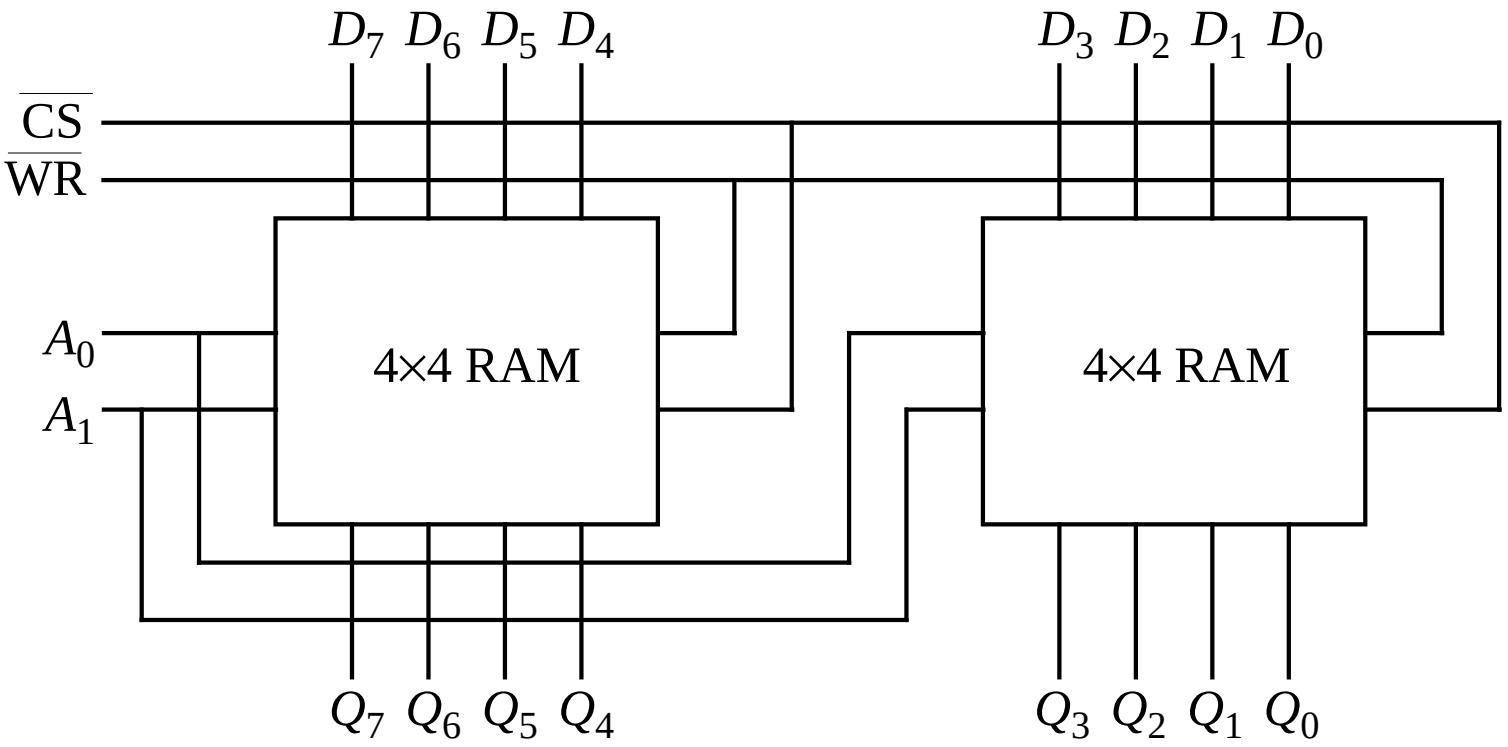


Enable = 1					
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

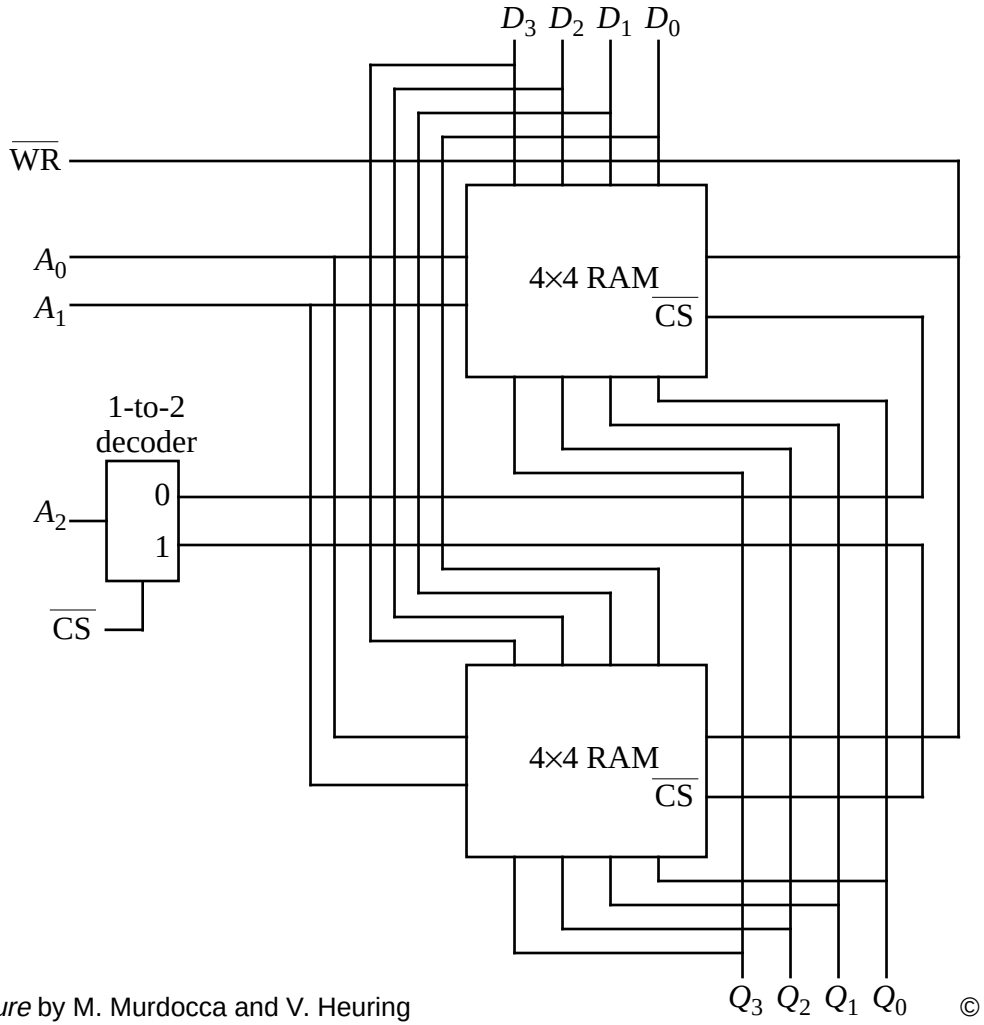
Enable = 0					
A	B	D_0	D_1	D_2	D_3
0	0	0	0	0	0
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0

$$D_0 = \overline{A}\,\overline{B} \qquad D_1 = \overline{A}\,B \qquad D_2 = A\,\overline{B} \qquad D_3 = A\,B$$

Two Four-Word by Four-Bit RAMs are Used in Creating a Four-Word by Eight-Bit RAM



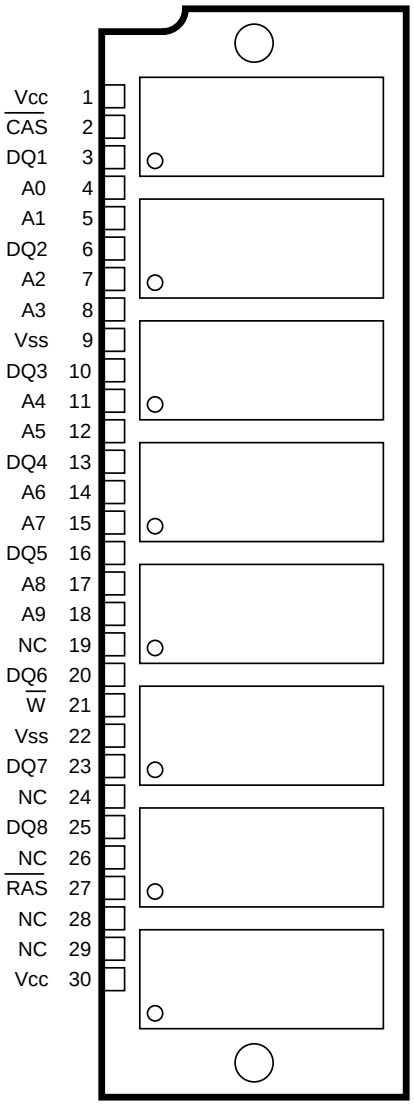
Two Four-Word by Four-Bit RAMs Make up an Eight-Word by Four-Bit RAM



Single-In-Line Memory Module

- **Adapted from(Texas Instruments, *MOS Memory: Commercial and Military Specifications Data Book*, Texas Instruments, Literature Response Center, P.O. Box 172228, Denver, Colorado, 1991.)**

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{cc}	5-V Supply
V_{ss}	Ground
$\overline{W}$	Write Enable

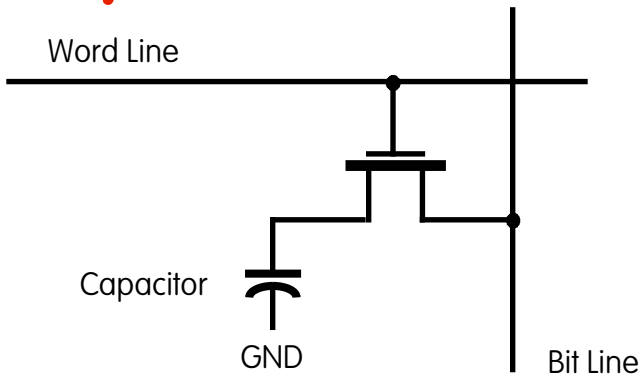


Types of Random Access Memory

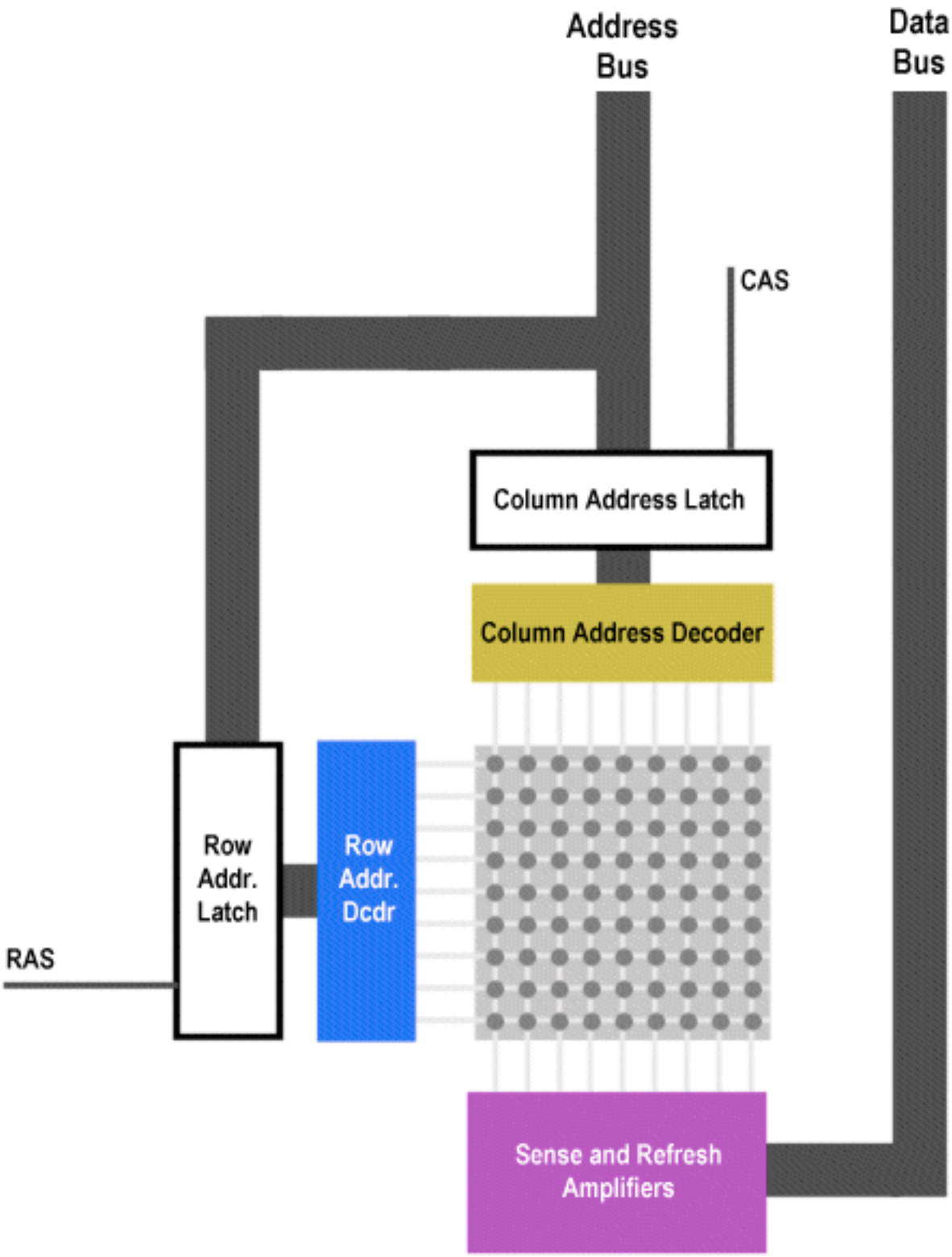
- **Static RAM (SRAM)**
  - Each bit is stored in a type of flip-flop
  - Typically takes four or six transistors per bit
  - Faster, but takes up more space in a chip
  - Retains information as long as power is supplied
  - Not to be confused with flash memory in digital cameras (EEPROMs)
- **Dynamic RAM (DRAM)**
  - Each bit is stored in a capacitor
  - Uses one capacitor and one transistor per bit
  - Slower, but takes up less space in a chip
  - Must be refreshed periodically (milliseconds), since the capacitor leaks

DRAM

- A DRAM memory cell



- Word line selects cell for reading or writing
- To write, the bit line is charged with logic 1 or 0
- To read, sensitive amplifier circuits detect small changes in bit line.
- Reading discharges the capacitor.

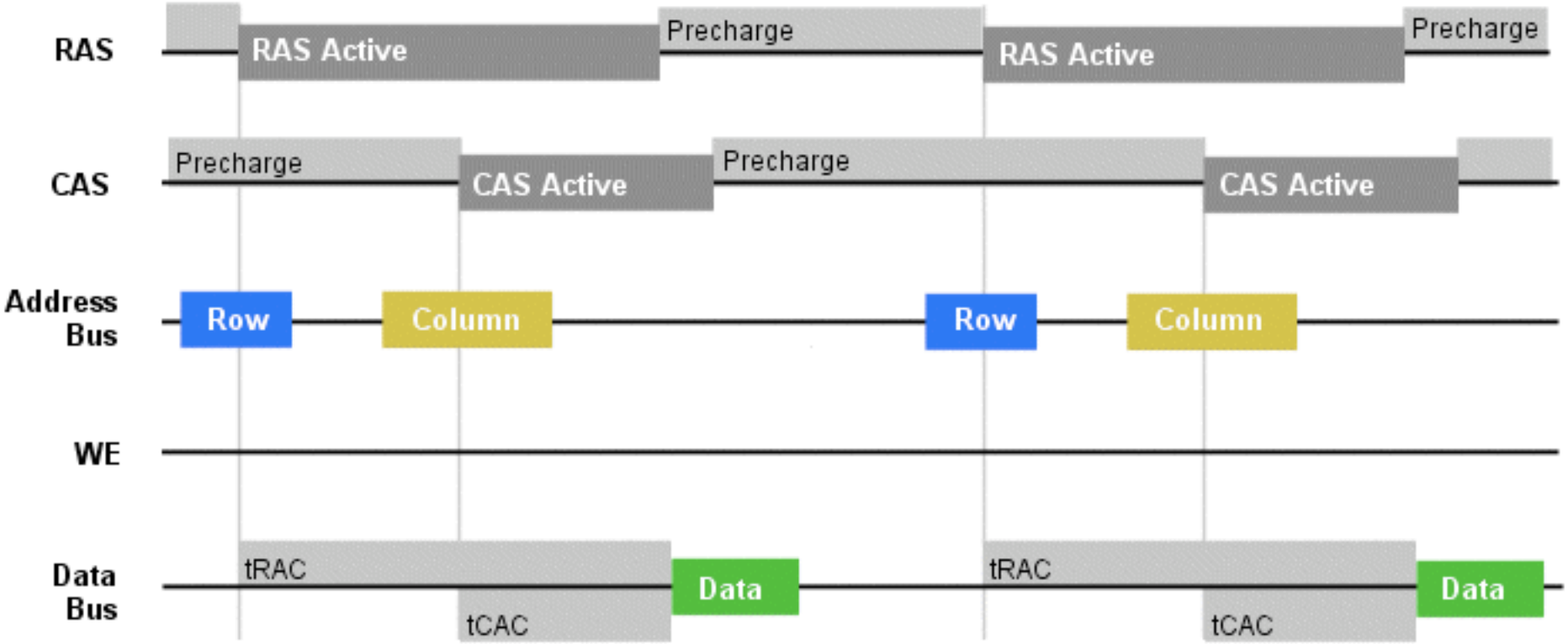


DRAM Read Cycle

1. Row address placed on the address bus.
2. Row Address Strobe (RAS) is asserted, allowing the row address to latch.
3. Row address decoder selects proper row.
4. Write Enable (WE) disabled.
5. Column address placed on the address bus.
6. Column Address Strobe (CAS) is activated, allowing the column address to latch.
7. Once the CAS signal has stabilized, sensing amplifiers places data from the selected row & column on data bus.
8. RAS and CAS deactivated. Cycle begins again.

http://www.arstechnica.com/paedia/r/ram_guide/figure1.2.gif

DRAM Read

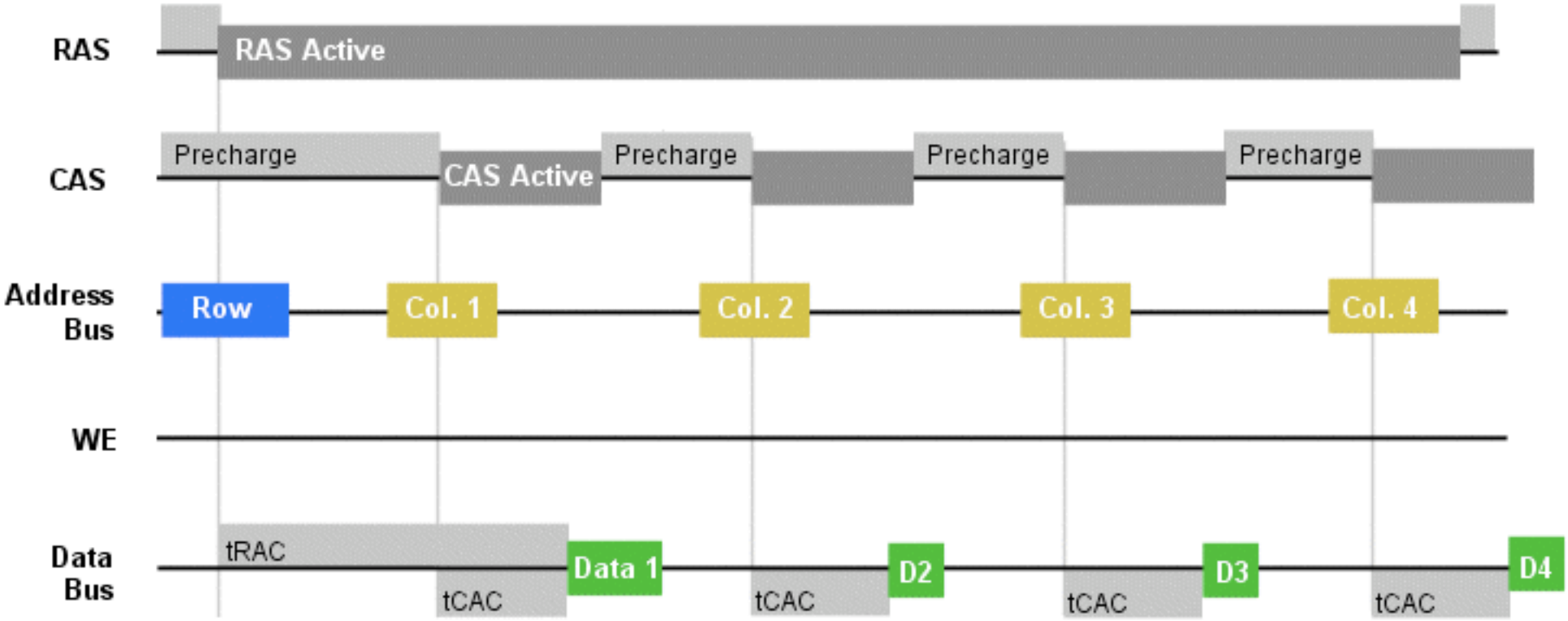


DRAM

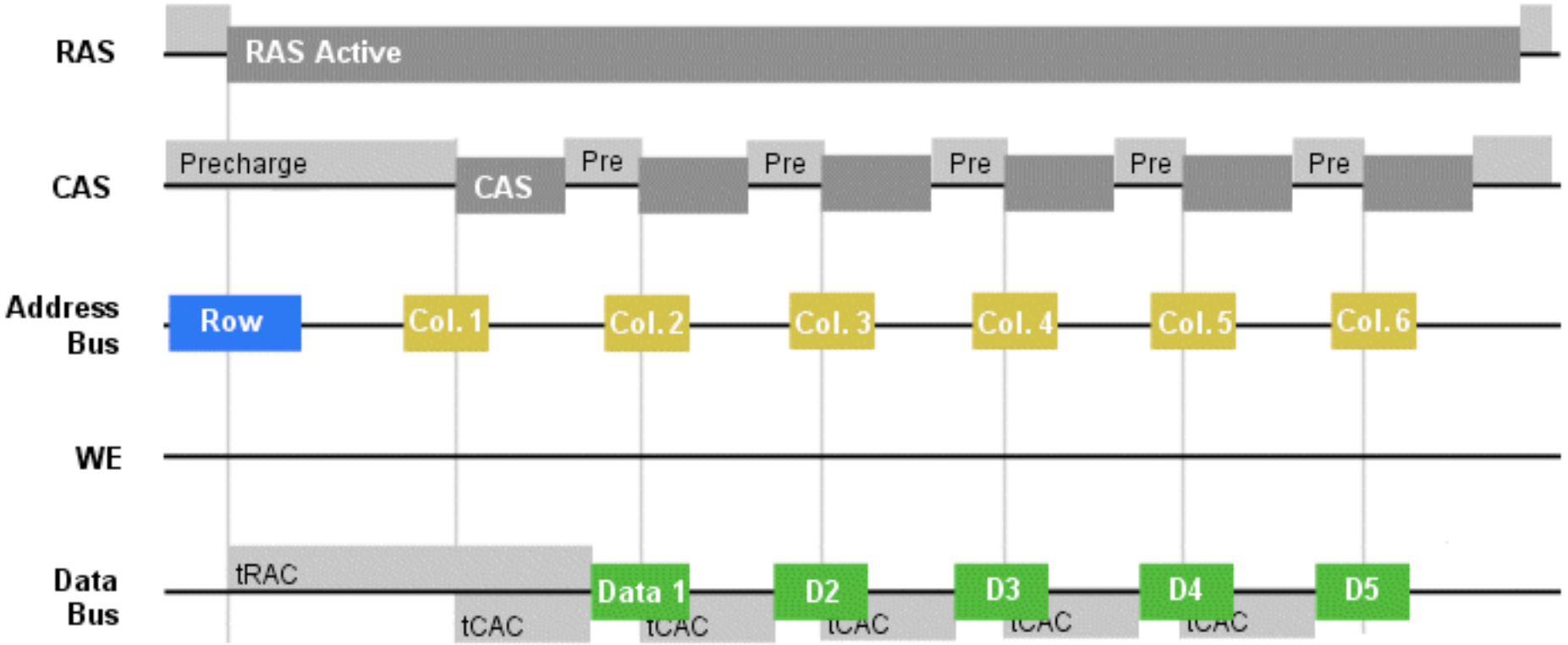
- DRAM is asynchronous, ignores system bus clock.
  - tRAC = Row Access Time = delay from RAS assertion until data is ready
  - tCAC = Column Access Time = delay from CAS assertion until data is ready
- DRAM access is slooooooow
- Each memory access must wait for time it takes to activate and deactivate RAS.
- Fast Page Mode (FPM) DRAM allows successive reads from the same row without deactivating RAS.
- Extended Data Out (EDO) DRAM overlaps CAS assertion and data reads.

http://www.arstechnica.com/paedia/r/ram_guide/figure2.2.gif

Fast Page Mode Read



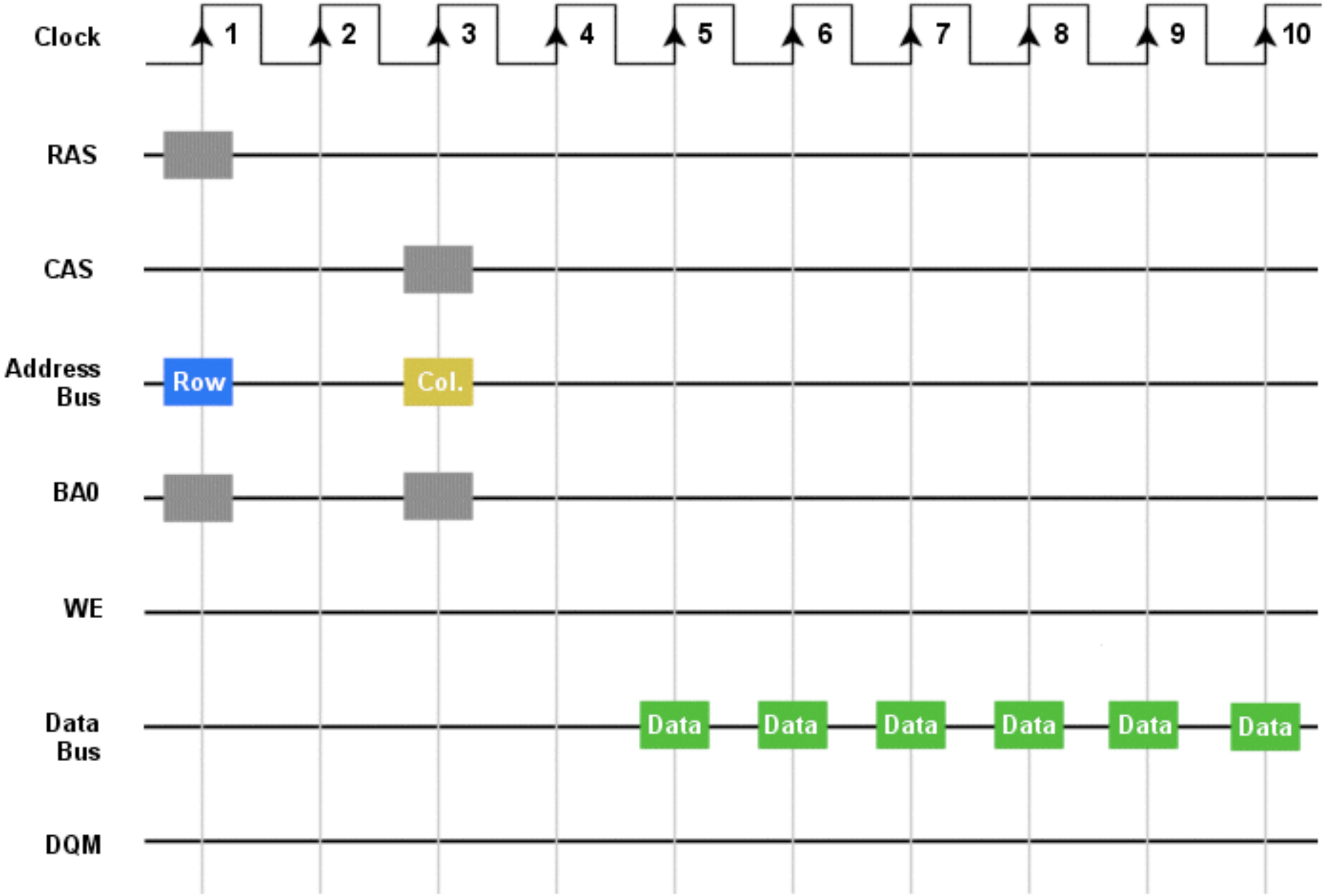
EDO Read


RAS
RAS Active
CAS
Precharge
CAS
Pre
Pre
Pre
Pre
Pre
Address Bus
Row
Col. 1
Col. 2
Col. 3
Col. 4
Col. 5
Col. 6
WE
Data Bus
tRAC
tCAC
Data 1
D2
D3
D4
D5

Synchronous DRAM (SDRAM)

- Uses system bus clock.
- Current models run at 433MHz (still much slower than CPU).
- Burst mode allows fast successive reads from the same row. (Good way to read in a cache line!)
- Double Data Rate (DDR) SDRAM provides data on the positive and negative edges of the clock.

SDRAM Read



Next Time

- Cache Memory