Name:_____

Question	Points
I.	/26
II.	/24
III.	/50
TOTAL:	/100

Instructions:

1. This is a closed-book, closed-notes exam.
2. You have 120 minutes for the exam.
3. Calculators are not allowed.
4. Show all of your work.
5. Clearly indicate your final answer.
6. A crib sheet with some properties of Boolean Algebra is included.

I. Multiple Choice (2 points each)

For each question in this section, circle **1** answer. Choose the **best** answer.

1. Which of the following sets of logic gates is universal?

   (a) { AND, NOT }
   (b) { AND, OR }
   (c) { OR }
   (d) { NOT }

2. In CMOS logic, a 2-input NAND gate can be constructed with

   (a) 1 transistor.
   (b) 4 transistors.
   (c) 12 transistors.
   (d) about 100 transistors.

3. A *semiconductor* is

   (a) a material composed of 50% conducting and 50% insulating materials.
   (b) grouped into three types: n-type, o-type and p-type.
   (c) used mostly to make tri-state buffers.
   (d) doped with impurities to affect its electrical properties.

4. The *propagation delay* of a combinational logic circuit is the period of time between

   (a) the positive edge and the negative edge of a clock cycle.
   (b) successive changes in the user input.
   (c) when the input changes and when the output becomes stable.
   (d) when an engineer is finished with the circuit's design and when the circuit is mass produced.

5. In general, finding the smallest equivalent combinational logic circuit with n input signals

   (a) can be done quickly using the Quine-McCluskey algorithm.
   (b) can be done quickly using the Karnaugh Map algorithm.
   (c) can be done quickly using the state reduction algorithm.
   (d) none of the above.

6. The purpose of the *flip-flops* in a finite state machine is to

   (a) synchronize the phases of a two-phase clock.
   (b) record the state of the finite state machine.
   (c) separate the odd and even states of the finite state machine.
   (d) separate the input and output states of the finite state machine.

7. A *glitch* occurs in a circuit when

   (a) there is an unwanted state or output, often as a result of a hazard.
   (b) the clock misses a cycle.
   (c) two wires that cross each other are mistakenly connected.
   (d) all of the above.

8. To record a 1 in a *positive-edge triggered* D flip-flop, the input must be held high:

   (a) while the clock signal is high.
   (b) while the clock signal is low.
   (c) before the clock signal goes from low to high.
   (d) before the clock signal goes from high to low.

9. A J-K flip-flop is placed in an endless toggle when

   (a) when J is high and K is low.
   (b) when J is low and K is high.
   (c) both J and K are low.
   (d) both J and K are high.

10. The two-phase clock in a master-slave J-K flip flop is used to

    (a) enable the master flip-flop before the slave flip-flop is enabled.
    (b) enable the slave flip-flop before the master flip-flop is enabled.
    (c) disable the master or slave flip-flop before the other flip-flop is enabled.
    (d) enable the master or the slave flip-flop before the other flip-flop is disabled.

11. The difference between a Mealy finite state machine and a Moore finite state machine is:

    (a) the output of a Moore machine depends only on the input whereas the output of a Mealy machine depends on the input and the state.

    (b) the output of a Moore machine depends only on the state of the machine whereas the output of a Mealy machine depends on the state and the input.

    (c) the Moore model uses J-K flip-flops and the Mealy model uses D flip-flops.

    (d) the Moore model uses a two-phase clock and the Mealy model uses a one-phase clock.

12. A *tri-state buffer* can be used to

    (a) temporarily disconnect a component from the rest of the circuitry.

    (b) store three values: -1, 0 and 1.

    (c) construct a Mod-3 counter.

    (d) store data in a shift register.

13. The difference between dynamic RAM and static RAM is that

    (a) dynamic RAM must be refreshed periodically.

    (b) static RAM is slower but much cheaper.

    (c) dynamic RAM is used in cache memory.

    (d) a dynamic RAM cell uses a flip-flop whereas static RAM cell uses a capacitor.

II. Short Answers (4 points each)

For each question in this section, *show all of your work.* Clearly indicate your final answer.

1. Explain the difference between combinational logic and sequential logic.

2. Name one advantage and one disadvantage of a carry lookahead adder in contrast to a ripple-carry adder.

3. Use the properties of Boolean Algebra to show that

$$\overline{A(B+C)+\overline{A}B} = \overline{B}(\overline{A}+\overline{C}).$$

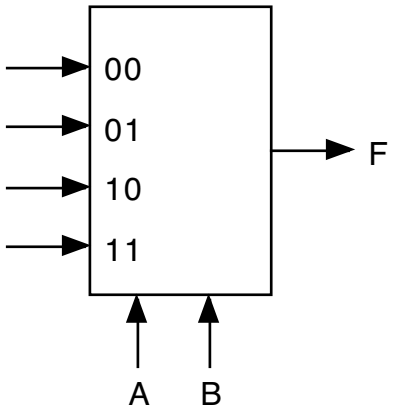
Label each step of your derivation with the name of the postulate or theorem used.

4. Fill in the truth table entries for the following Boolean formula. Then, write down its canonical Product-of-Sums Boolean formula. Do not simplify the formula.

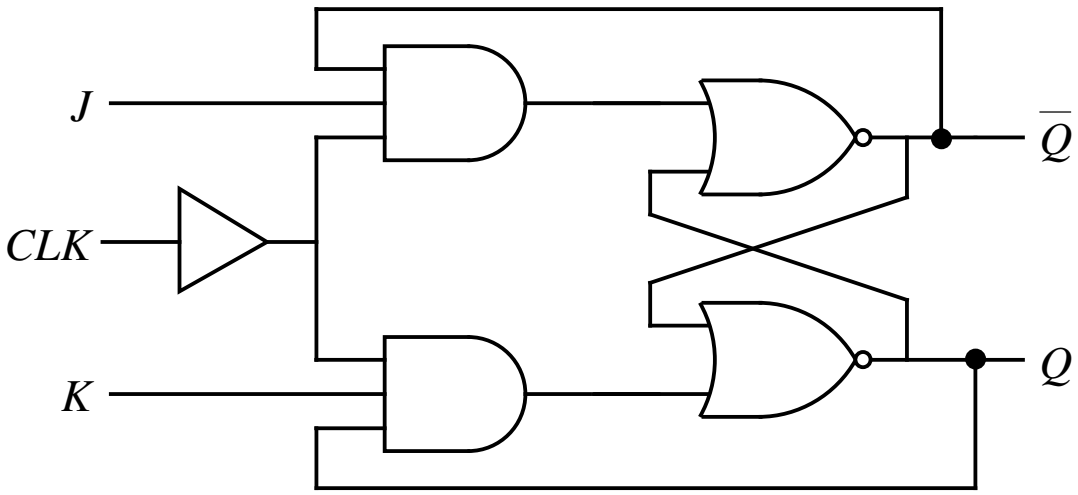
$$f(X,Y,Z) = XY + \overline{X}Z + X\overline{Z}$$

X	Y	Z	XY	$\overline{X}Z$	$X\overline{Z}$	$f(X,Y,Z)$
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

5. Use a single 4-to-1 MUX to implement the function $f(X, Y, Z) = \overline{X}\,\overline{Y}Z + Y\overline{Z}$. In the diagram for a 4-to-1 MUX below, indicate what values should be given to the data inputs and the control inputs. Show your work. Assume that $\overline{X}$, $\overline{Y}$ and $\overline{Z}$ are also available.



6. Consider the J-K flip-flop shown below. Suppose that the clock is low and the current inputs are $J = 0$ and $K = 0$. Furthermore, suppose that the current outputs are $Q = 0$ and $\overline{Q} = 1$. Label the inputs and output of each gate in the diagram if $J = 1$ and $K = 0$ when the clock goes high. *Note:* the clock signal is attached to a buffer, *not* an inverter.

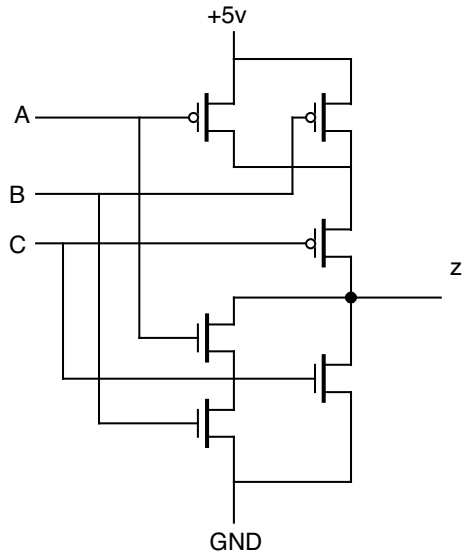


III. Problems (50 points total)

1. **CMOS circuits (12 points).** For the CMOS circuit below,

   (a) Provide a Boolean formula for the circuit. You may use any method you prefer (inspection, truth table, ...) as long as the resulting Boolean formula is equivalent to the circuit.

   (b) Draw a circuit diagram of the formula using AND, OR and NOT gates.



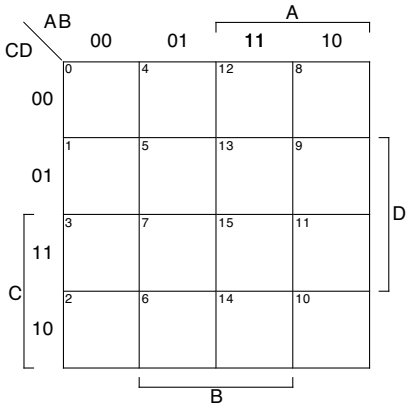
2. **Karnaugh Maps (12 points).** Using the Karnaugh maps provided, give a minimum Sum-of-Products or Product-of-Sums Boolean formula for each of the following Boolean functions.

(a) $f(A, B, C, D) = \sum m(0, 1, 2, 3, 6, 9, 14)$

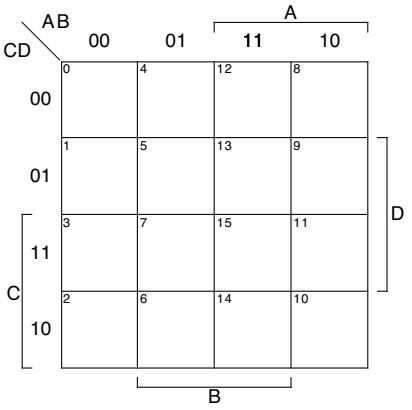
(b) $f(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 7, 14)$

(c) $f(A, B, C, D) = \sum m(1, 3, 4, 7, 11) + d(5, 12, 13, 14, 15)$

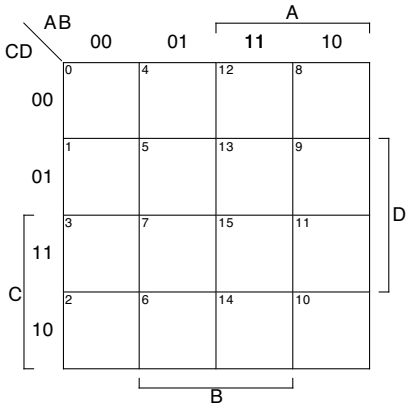
(d) $f(A, B, C, D) = \sum m(7, 8, 13, 15) + d(3, 10, 12, 14)$



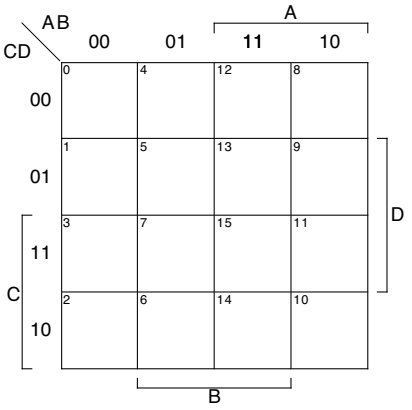
(a) $f(A, B, C, D) =$



(b) $f(A, B, C, D) =$



(c) $f(A, B, C, D) =$



(d) $f(A, B, C, D) =$

3. **State Reduction (12 points).** Use the state reduction algorithm to construct a minimum-state finite state machine (FSM) equivalent to the FSM given by the state transition table below. (The FSM given is a Mealy machine.) Draw the state transition diagram (with circles and arrows) for the reduced FSM. Be sure to indicate which old states are grouped together to form the new states.

	0	1
A	B/0	E/0
B	C/0	B/0
C	B/0	G/0
D	B/0	D/0
E	F/0	E/0
F	C/0	B/0
G	F/0	D/1

	B	C	D	E	F	G
A						
B	-					
C	-	-				
D	-	-	-			
E	-	-	-	-		
F	-	-	-	-	-	

4. **Finite State Machines with J-K flip flops (14 points).**

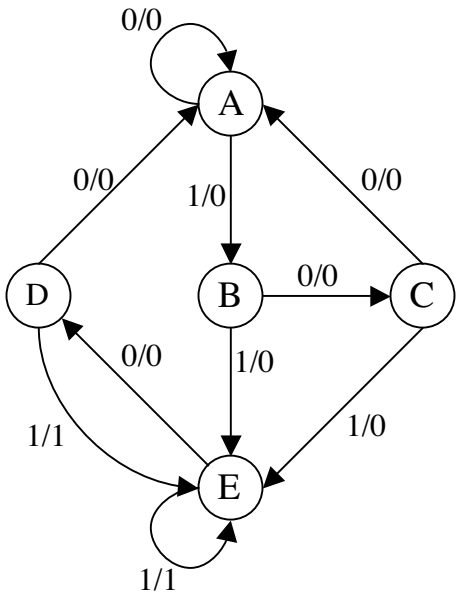
Consider the transition diagram for a finite state machine below. Use the state assignments:

A = 000, B = 001, C = 011, D = 100 and E = 101.

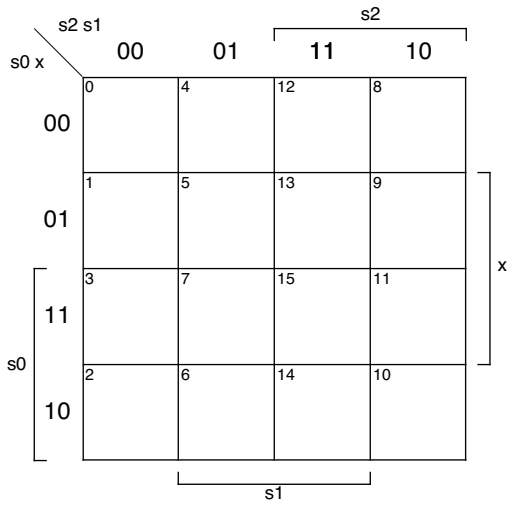
Here x and z are the input and output, respectively. The columns j_2, k_2, j_1, k_1, j_0 and k_0 are the inputs to three J-K flip-flops that hold the state bits s_2, s_1 and s_0 respectively. Fill in the truth table below. Then use the Karnaugh maps on the next page to derive the Boolean formulas for j_2, k_2, j_1, k_1, j_0 and k_0.

J-K Excitation Table

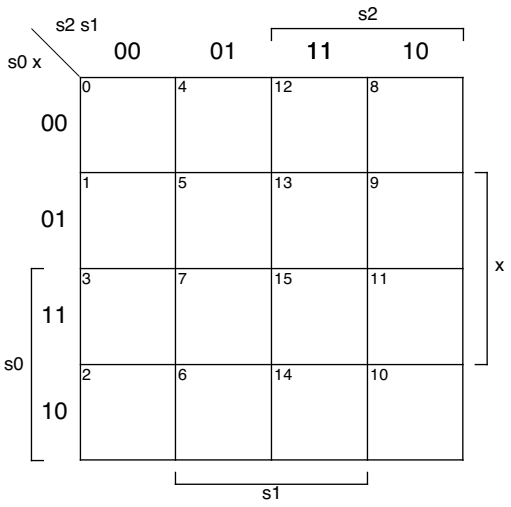
Q	Q'	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0



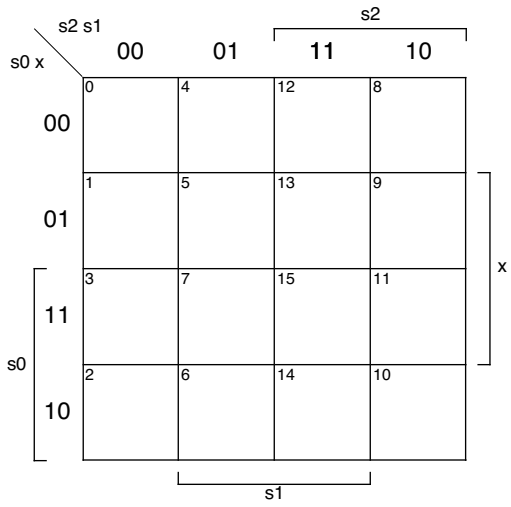
	s_2	s_1	s_0	x	s_2'	s_1'	s_0'	z	j_2	k_2	j_1	k_1	j_0	k_0
0	0	0	0	0										
1	0	0	0	1										
2	0	0	1	0										
3	0	0	1	1										
4	0	1	0	0										
5	0	1	0	1										
6	0	1	1	0										
7	0	1	1	1										
8	1	0	0	0										
9	1	0	0	1										
10	1	0	1	0										
11	1	0	1	1										
12	1	1	0	0										
13	1	1	0	1										
14	1	1	1	0										
15	1	1	1	1										



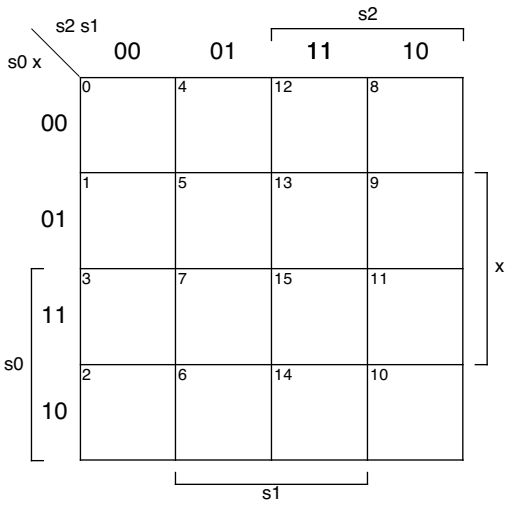
$j_2 =$



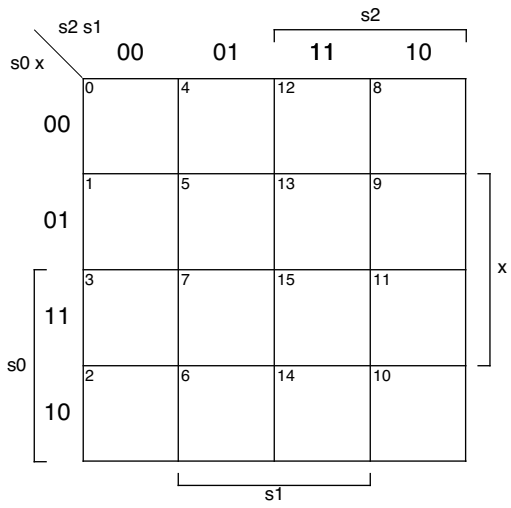
$k_2 =$



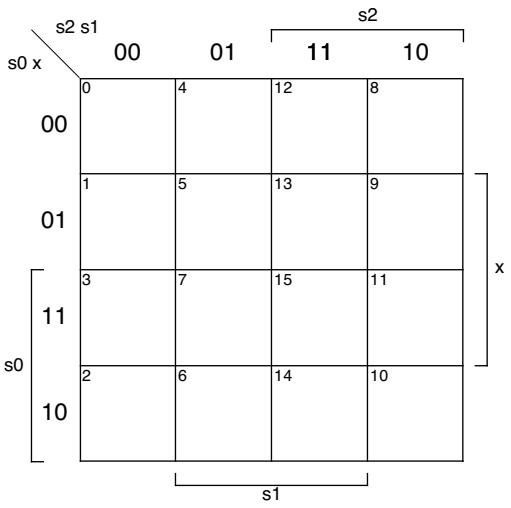
$j_1 =$



$k_1 =$



$j_0 =$



$k_0 =$