

CMSC 313 Lecture 26

- **Review FSM Simplification**
- **Using J-K Flip-Flops**
- **DigSim Exercise 2**

Simplifying Finite State Machines

- **State Reduction: equivalent FSM with fewer states**
- **State Assignment: choose an assignment of bit patterns to states (e.g., A is 010) that results in a smaller circuit**
- **Choice of flip-flops: use D flip-flops, J-K flip-flops or a T flip-flops? a good choice could lead to simpler circuits.**

Last Time

- **State Reduction Algorithm**
- **State Assignment Heuristics**
- **Used Sequence Detector example:**
 - ◇ **Reduced number of states from 7 to 6**
 - ◇ **Better state assignment yielded smaller circuit**

Excitation Tables

- Each table shows the settings that must be applied at the inputs at time t in order to change the outputs at time $t+1$.

*S-R
flip-flop*

Q_t	Q_{t+1}	S	R
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

*D
flip-flop*

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

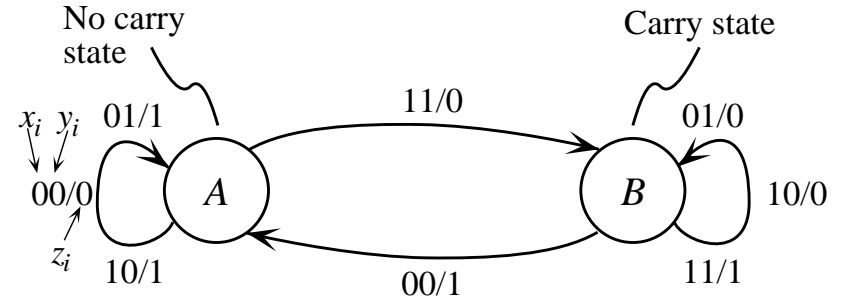
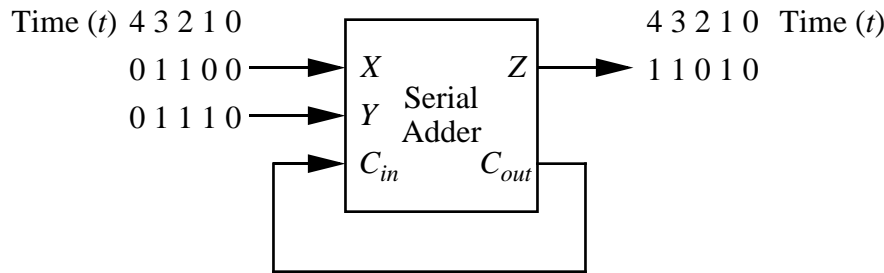
*J-K
flip-flop*

Q_t	Q_{t+1}	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

*T
flip-flop*

Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Serial Adder



- **State transition diagram, state table, and state assignment for a serial adder.**

	Input	XY			
Present state		00	01	10	11
A		A/0	A/1	A/1	B/0
B		A/1	B/0	B/0	B/1

Next state Output

	Input	XY			
Present state (S_i)		00	01	10	11
A:0		0/0	0/1	0/1	1/0
B:1		0/1	1/0	1/0	1/1

Serial Adder Next-State Functions

- Truth table showing next-state functions for a serial adder for D, S-R, T, and J-K flip-flops. Shaded functions are used in the example.

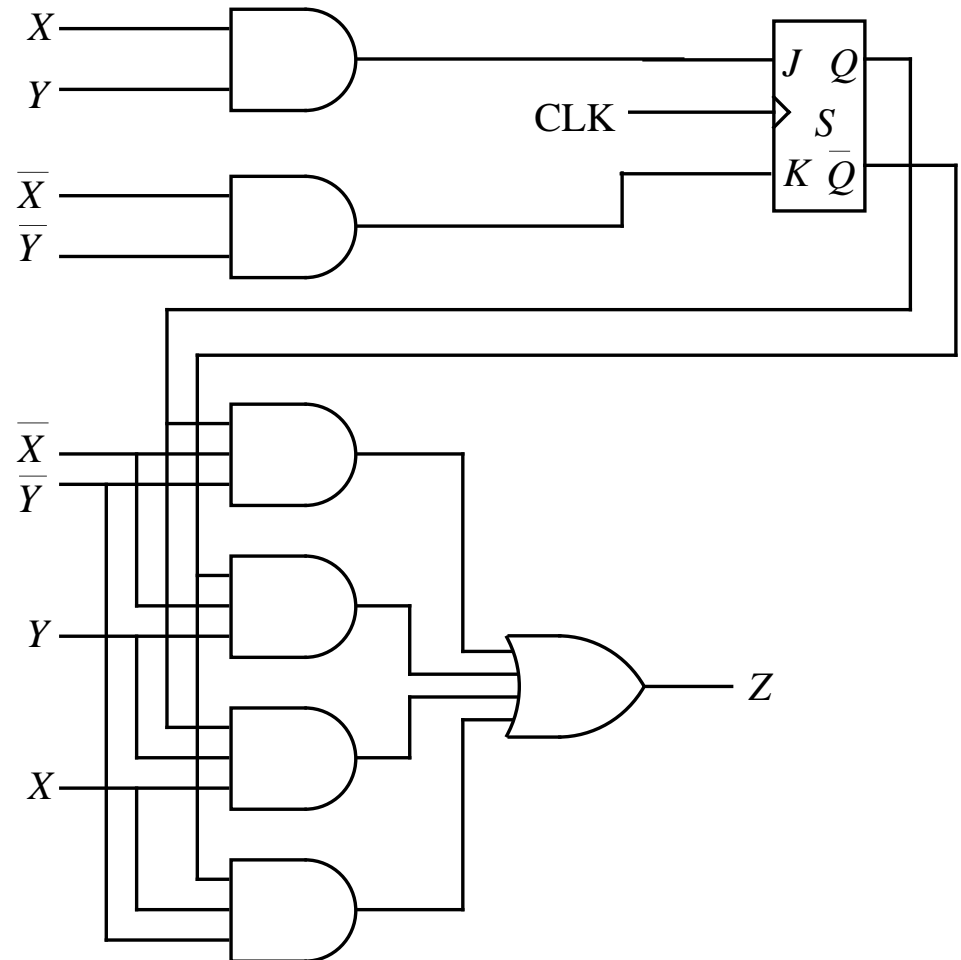
Present State			(Set) (Reset)						
<i>X</i>	<i>Y</i>	<i>S_t</i>	<i>D</i>	<i>S</i>	<i>R</i>	<i>T</i>	<i>J</i>	<i>K</i>	<i>Z</i>
0	0	0	0	0	0	0	0	<i>d</i>	0
0	0	1	0	0	1	1	<i>d</i>	1	1
0	1	0	0	0	0	0	0	<i>d</i>	1
0	1	1	1	0	0	0	<i>d</i>	0	0
1	0	0	0	0	0	0	0	<i>d</i>	1
1	0	1	1	0	0	0	<i>d</i>	0	0
1	1	0	1	1	0	1	1	<i>d</i>	0
1	1	1	1	0	0	0	<i>d</i>	0	1

J-K Flip-Flop Serial Adder Circuit

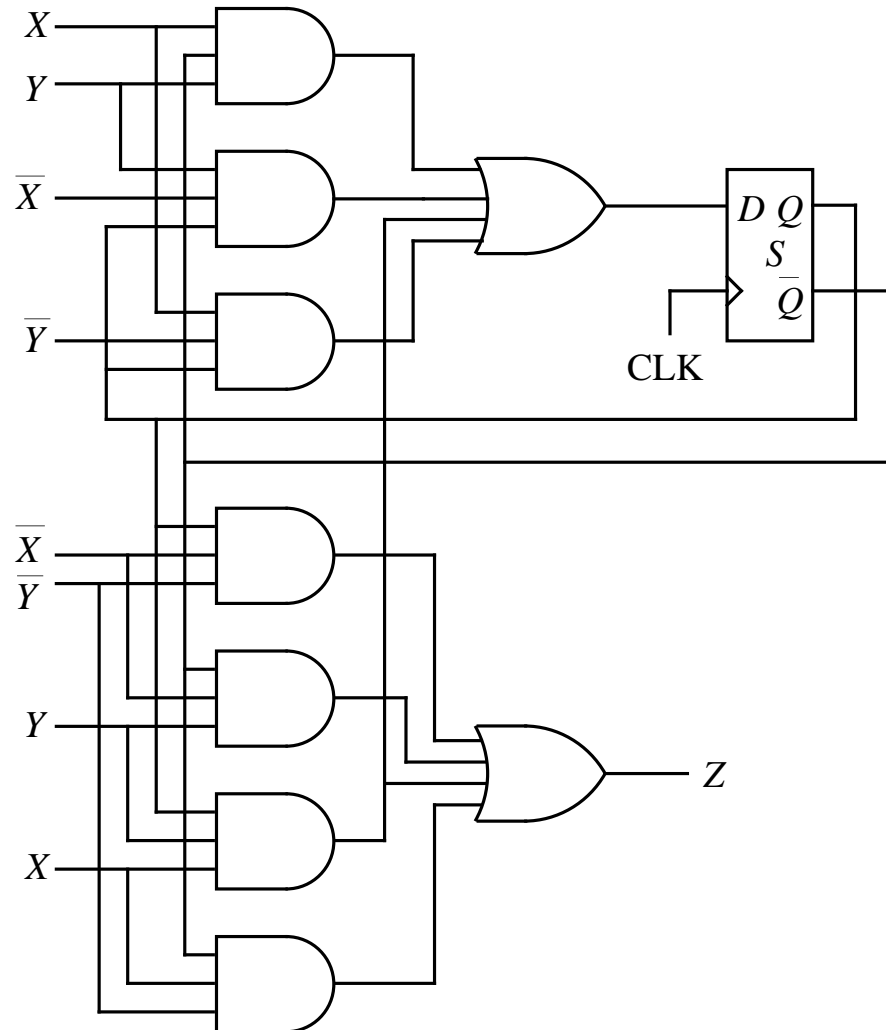
$$J = XY$$

$$K = \bar{X}\bar{Y}$$

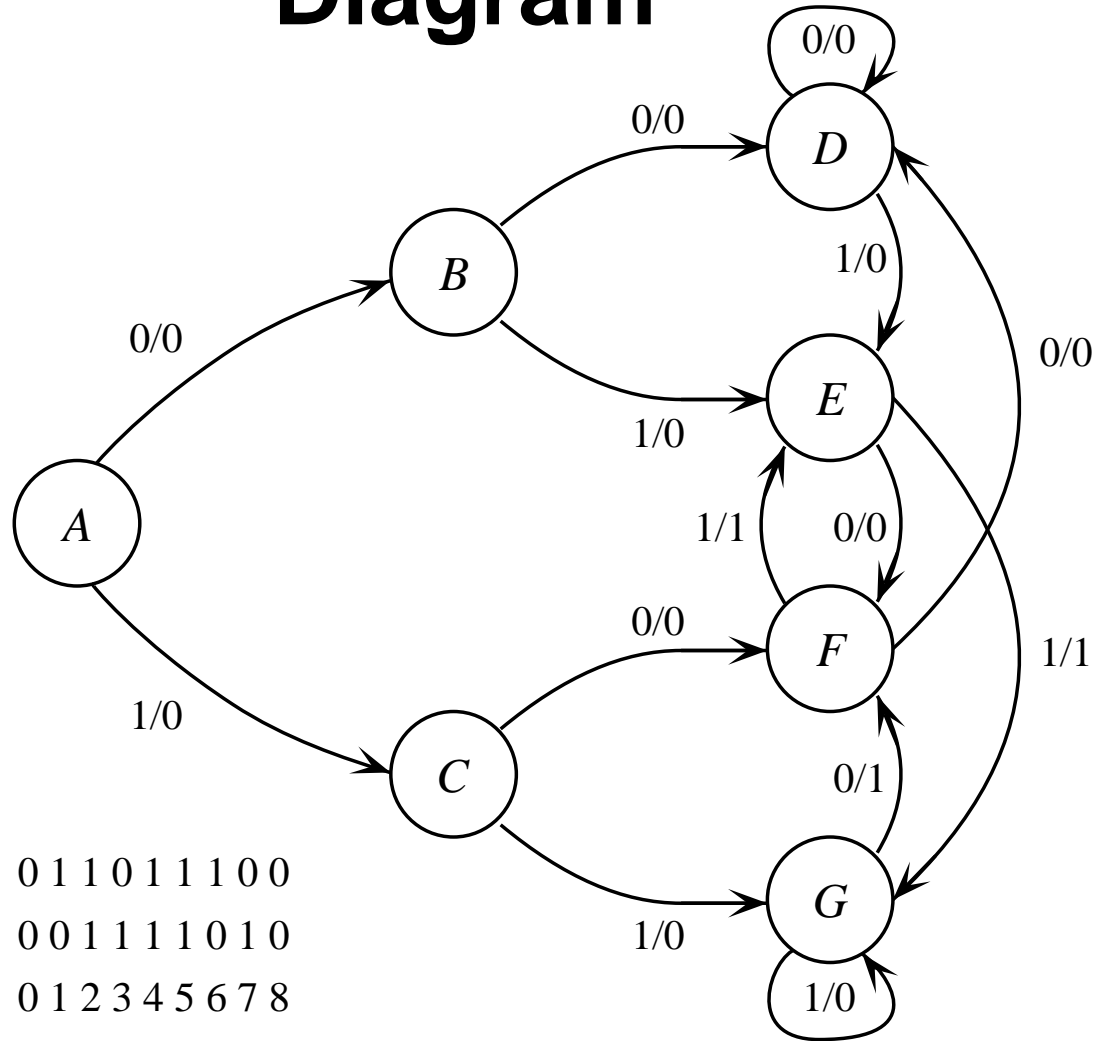
$$Z = \bar{X}\bar{Y}S + \bar{X}Y\bar{S} + XY\bar{S} + X\bar{Y}S$$



D Flip-Flop Serial Adder Circuit

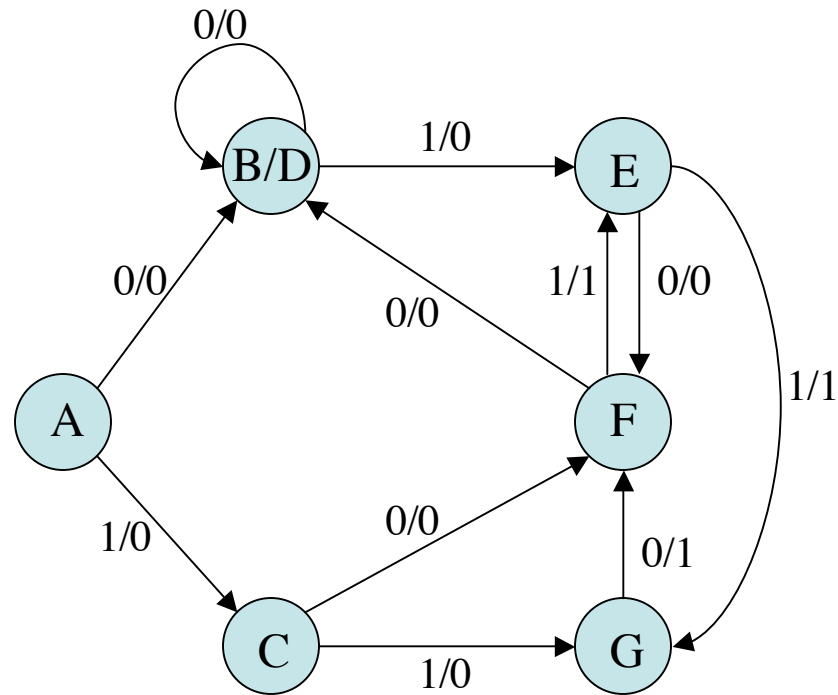


Sequence Detector State Transition Diagram



Input: 0 1 1 0 1 1 1 0 0
 Output: 0 0 1 1 1 1 0 1 0
 Time: 0 1 2 3 4 5 6 7 8

6-State Sequence Detector



Improved Sequence Detector?

- **Formulas from the 7-state FSM:**

$$s2' = (\overline{s0} + x) (s2 + s1 + s0)$$

$$s1' = \overline{s0} x + s0 \overline{x} = s0 \text{ xor } x$$

$$s0' = \overline{x}$$

$$z = s2 \overline{s1} x + s2 s1 \overline{x}$$

- **Formulas from the 6-state FSM:**

$$s2' = s2 s0 + s1$$

$$s1' = \overline{s2} \overline{s1} x + s2 \overline{s0} x$$

$$s0' = \overline{s2} \overline{s1} \overline{x} + s0 x + s2 \overline{s0} + s1 x$$

$$z = s2 \overline{s0} x + s1 s0 x + s2 s0 \overline{x}$$

Sequence Detector State Assignment

7-state

	s2	s1	s0	x	s2'	s1'	s0'	z
0	0	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	1	0
3	0	0	1	1	1	0	0	0
4	0	1	0	0	1	0	1	0
5	0	1	0	1	1	1	0	0
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	1	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	0	1	1	0
11	1	0	1	1	1	0	0	1
12	1	1	0	0	1	0	1	1
13	1	1	0	1	1	1	0	0
14	1	1	1	0	d	d	d	d
15	1	1	1	1	d	d	d	d

A = 000
 B = 001
 C = 010
 D = 011

E = 100
 F = 101
 G = 110

new 6-state

	s2	s1	s0	x	s2'	s1'	s0'	z
0	0	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	0	1	0
3	0	0	1	1	1	0	0	0
4	0	1	0	0	1	0	1	0
5	0	1	0	1	1	1	0	0
6	0	1	1	0	d	d	d	d
7	0	1	1	1	d	d	d	d
8	1	0	0	0	1	0	1	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	0	0	1	0
11	1	0	1	1	1	0	0	1
12	1	1	0	0	1	0	1	1
13	1	1	0	1	1	1	0	0
14	1	1	1	0	d	d	d	d
15	1	1	1	1	d	d	d	d

A = 000
 B/D = 001
 C = 010
~~D = 011~~

E = 100
 F = 101
 G = 110

Improved Sequence Detector

- **Textbook formulas for the 6-state FSM:**

$$s2' = s2 s0 + s1$$

$$s1' = \overline{s2} \overline{s1} x + s2 \overline{s0} x$$

$$s0' = \overline{s2} \overline{s1} \overline{x} + s0 x + s2 \overline{s0} + s1 x$$

$$z = s2 \overline{s0} x + s1 s0 x + s2 s0 \overline{x}$$

- **New formulas for the 6-state FSM:**

$$s2' = (\overline{s0} + x) (s2 + s1 + s0)$$

$$s1' = \overline{s0} x$$

$$s0' = \overline{x}$$

$$z = s2 \overline{s1} x + s2 s1 \overline{x}$$

6-State Sequence Detector

	s2	s1	s0	x	s2'	s1'	s0'	z	j2	k2	j1	k1	j0	k0
0	0	0	0	0	0	0	1	0	0	<i>d</i>	0	<i>d</i>	1	<i>d</i>
1	0	0	0	1	0	1	0	0	0	<i>d</i>	1	<i>d</i>	0	<i>d</i>
2	0	0	1	0	0	0	1	0	0	<i>d</i>	0	<i>d</i>	<i>d</i>	0
3	0	0	1	1	1	0	0	0	1	<i>d</i>	0	<i>d</i>	<i>d</i>	1
4	0	1	0	0	1	0	1	0	1	<i>d</i>	<i>d</i>	1	1	<i>d</i>
5	0	1	0	1	1	1	0	0	1	<i>d</i>	<i>d</i>	0	0	<i>d</i>
6	0	1	1	0	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>
7	0	1	1	1	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>
8	1	0	0	0	1	0	1	0	<i>d</i>	0	0	<i>d</i>	1	<i>d</i>
9	1	0	0	1	1	1	0	1	<i>d</i>	0	1	<i>d</i>	0	<i>d</i>
10	1	0	1	0	0	0	1	0	<i>d</i>	1	0	<i>d</i>	<i>d</i>	0
11	1	0	1	1	1	0	0	1	<i>d</i>	0	0	<i>d</i>	<i>d</i>	1
12	1	1	0	0	1	0	1	1	<i>d</i>	0	<i>d</i>	1	1	<i>d</i>
13	1	1	0	1	1	1	0	0	<i>d</i>	0	<i>d</i>	0	0	<i>d</i>
14	1	1	1	0	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>
15	1	1	1	1	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>

Q	Q'	J	K
0	0	0	<i>d</i>
0	1	1	<i>d</i>
1	0	<i>d</i>	1
1	1	<i>d</i>	0

6-State Sequence Detector

J2

s0 x		s2 s1		s2		
		00	01	11	10	
0	4	12	8	x		
00	0	1	d			d
1	5	13	9			
01	0	1	d			d
3	7	15	11	x		
11	1	d	d			d
2	6	14	10			
10	0	d	d			d
		s1				

$$J2 = s1 + s0 x$$

K2

s0 x		s2 s1		s2		
		00	01	11	10	
0	4	12	8	x		
00	d	d	0			0
1	5	13	9			
01	d	d	0			0
3	7	15	11	x		
11	d	d	d			0
2	6	14	10			
10	d	d	d			1
		s1				

$$K2 = s0 \bar{x}$$

6-State Sequence Detector

J1

		s2 s1		s2		
	s0 x	00	01	11	10	
	00	0	d	d	0	
	01	1	d	d	1	x
	11	0	d	d	0	
	10	0	d	d	0	
s0		s1				

$$J1 = \overline{s0} x$$

K1

		s2 s1		s2		
	s0 x	00	01	11	10	
	00	d	1	1	d	
	01	d	0	0	d	x
	11	d	d	d	d	
	10	d	d	d	d	
s0		s1				

$$K1 = \overline{x}$$

6-State Sequence Detector

J0

		s2 s1				s2	
	s0 x	00	01	11	10		
	00	0	4	12	8		
	01	1	5	13	9		
	11	3	7	15	11		
	10	2	6	14	10		
		s1					
						x	

The truth table for J0 shows the output for each combination of state bits s0, s1, and s2. The output is 1 for (s0, s1) pairs (00, 01), (11, 10), and 0 for (s0, s1) pairs (01, 11). All other combinations result in a don't care (d). A green rounded rectangle highlights the region where s0 = 01 and s1 = 11, which corresponds to the expression \overline{x} .

$$J0 = \overline{x}$$

K0

		s2 s1				s2	
	s0 x	00	01	11	10		
	00	0	4	12	8		
	01	1	5	13	9		
	11	3	7	15	11		
	10	2	6	14	10		
		s1					
						x	

The truth table for K0 shows the output for each combination of state bits s0, s1, and s2. The output is 1 for (s0, s1) pairs (11, 10) and (10, 00), and 0 for (s0, s1) pairs (01, 11) and (10, 10). All other combinations result in a don't care (d). A red rounded rectangle highlights the region where s0 = 01 and s1 = 11, which corresponds to the expression x.

$$K0 = x$$

Improved Sequence Detector

- **Formulas for the 6-state FSM with D Flip-flops:**

$$s2' = (\overline{s0} + x) (s2 + s1 + s0)$$

$$s1' = \overline{s0} x$$

$$s0' = \overline{x}$$

- **Formulas for the 6-state FSM with J-K Flip-flops:**

$$J2 = s1 + s0 x \quad K2 = s0 \overline{x}$$

$$J1 = \overline{s0} x \quad K1 = \overline{x}$$

$$J0 = \overline{x} \quad K0 = x$$

DigSim Assignment 2: Finite State Machine Simplifications

Due: Tuesday December 9, 2003

Objective

The objective is to design and simplify a moderately complex a finite state machine.

Assignment

For this project you will design and implement in DigSim a Mealy finite state machine with one input bit x and one output bit z . The machine's output z is 1 whenever the input sequence ...0111 or ...1000 has been detected. The patterns may overlap. For example, if the machine is given input 0111000, the output would be 0001001. [Adapted from *Contemporary Logic Design*, Randy H. Katz, Benjamin/Cummings Publishing, 1994.]

In order to complete the project, you must accomplish the following tasks. Note that for this project, you will submit both your design work (on paper) and the DigSim implementation of the resulting finite state machine (via submit).

1. Draw a transition diagram for the finite state machine described above. Use the state reduction algorithm to minimize the number of states in your machine. Although, you might start with an FSM with as many as 15 states, at the end of the reduction process you should have 7 states in your machine. Name your states A, B, C, D, E, F and G. You may take shortcuts, but you must show your work.
2. Assign bit patterns to each state of the machine. Use the heuristics for state assignment presented in class (available on the course lecture topics web page). Do this step carefully as it will have a large effect on the complexity of your final circuit. *Hint*: follow the loops in the FSM and try to assign bit patterns such that in each step of the loop only one state bit changes. You might not be able to achieve this for *every* step of the loop, but you can try to have only one state bit change for *most* steps of the loop. Write down your final state assignment in the table given.
3. Fill in the state transition table for the finite state machine given below. In this table, s_2 , s_1 and s_0 are the state bits, x is the input bit and z is the output bit. Then s_2' , s_1' and s_0' are the next states to be stored in the flip flops.
4. Use the Karnaugh maps provided to simplify the Boolean formulas for a finite state machine to be implemented using D flip-flops. You will need Karnaugh maps for s_2' , s_1' , s_0' and z .
5. Using the excitation table for J-K flip-flops, fill in the columns j_2 , k_2 , j_1 , k_1 , j_0 and k_0 in the truth table below. The columns j_2 and k_2 represent the settings to the inputs of the J-K flip-flop that will cause it to store the state bit s_2' . The columns j_1 , k_1 , j_0 and k_0 are analogous for the J-K flip-flops used to store state bits s_1 and s_0 .
6. Use the Karnaugh maps provided to simplify the Boolean formulas for the J and K inputs to each J-K flip flop. You will need Karnaugh maps for j_2 , k_2 , j_1 , k_1 , j_0 and k_0 . The formula for the output z will be the same as in Step 4.
7. Decide whether you want to use D flip-flops or J-K flip-flops. Briefly justify your choice.
8. Implement the resulting circuit in DigSim. *Hint*: it is possible to implement this FSM using fewer than 14 gates. If your circuit requires many more gates, redo the simplification steps.

What to submit

In class on Tuesday December 9, turn in your finite state diagram, truth table, Karnaugh maps and the resulting Boolean formulas on paper. Make copies of these, if you still need them to implement your circuit in DigSim.

Save your circuit as you did in DigSim Assignment 1. Submit the circuit file using the Unix submit command as in previous assignments. The submission name for this assignment is: `digsim2`.

CMSC 313 Digsim Exercise 2

Name: _____

Minimized 7-State Transition Diagram (show work)

State Assignment:

A	
B	
C	
D	
E	
F	
G	
unused	

Excitation Table for J-K Flip-Flops

Q	Q'	J	K
0	0	0	<i>d</i>
0	1	1	<i>d</i>
1	0	<i>d</i>	1
1	1	<i>d</i>	0

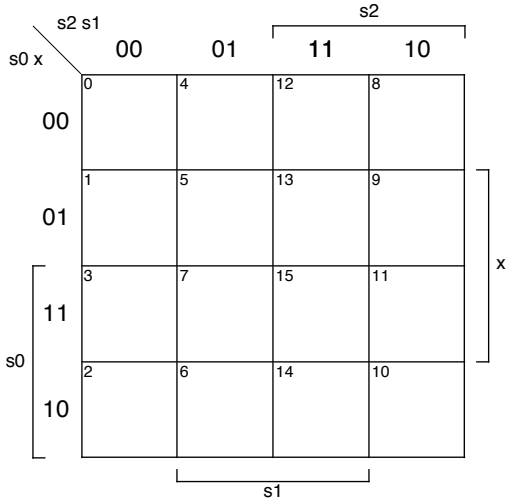
Truth Table:

	s2	s1	s0	x	s2'	s1'	s0'	z	j2	k2	j1	k1	j0	k0
0	0	0	0	0										
1	0	0	0	1										
2	0	0	1	0										
3	0	0	1	1										
4	0	1	0	0										
5	0	1	0	1										
6	0	1	1	0										
7	0	1	1	1										
8	1	0	0	0										
9	1	0	0	1										
10	1	0	1	0										
11	1	0	1	1										
12	1	1	0	0										
13	1	1	0	1										
14	1	1	1	0										
15	1	1	1	1										

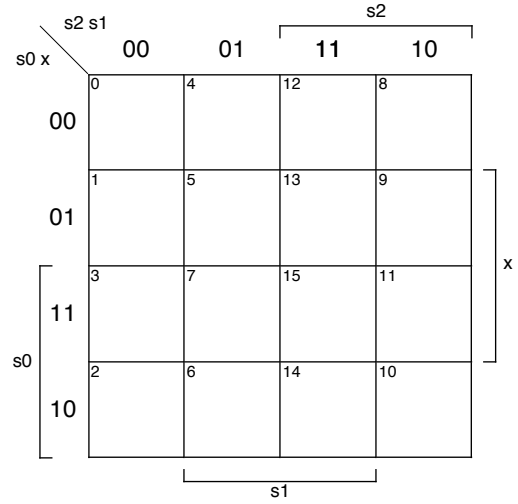
Question:

Should you use D flip-flops or J-K flip-flops to implement this circuit? Why?

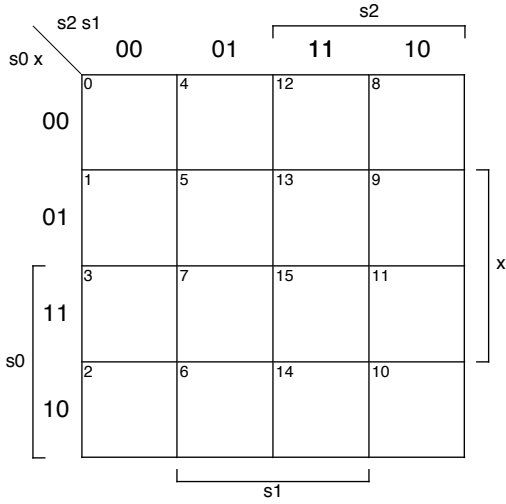
Karnaugh Maps for D Flip-Flops and the output



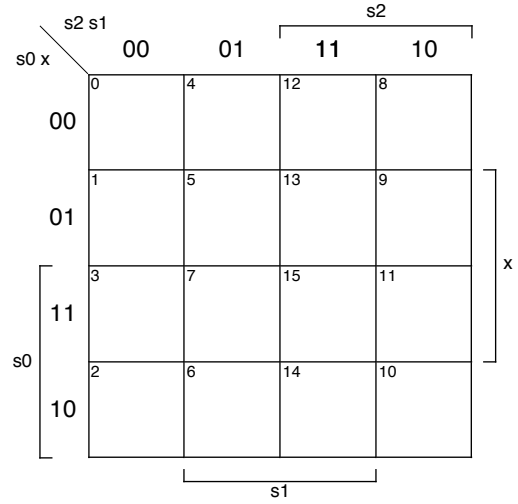
$s_2' =$



$s_1' =$

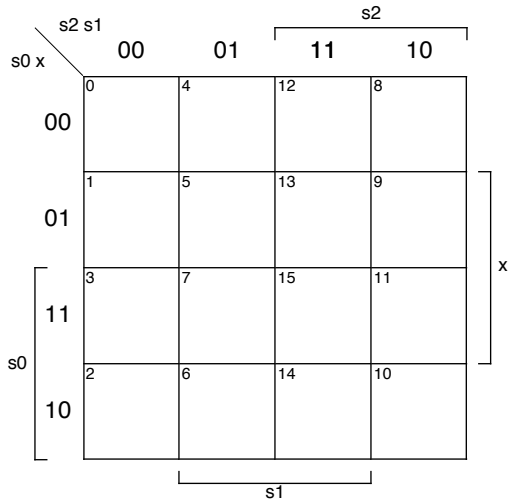


$s_0' =$

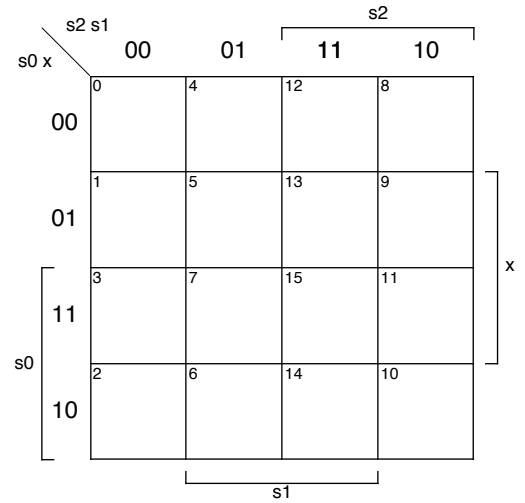


$Z =$

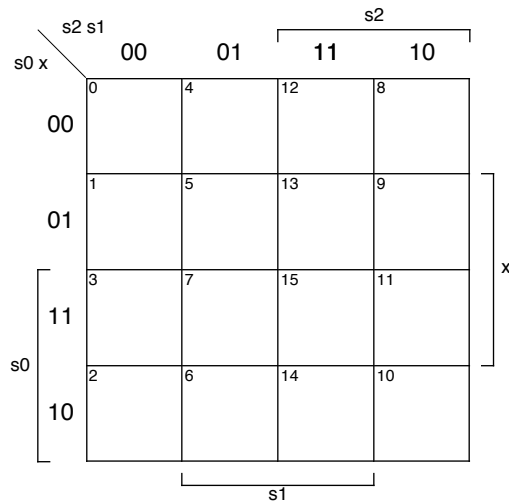
Karnaugh Maps for J-K Flip-Flops



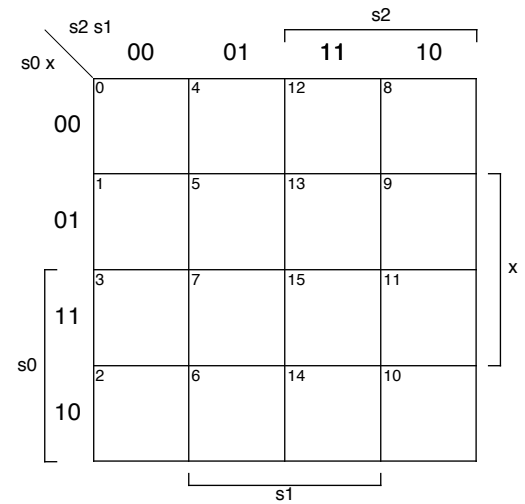
j2 =



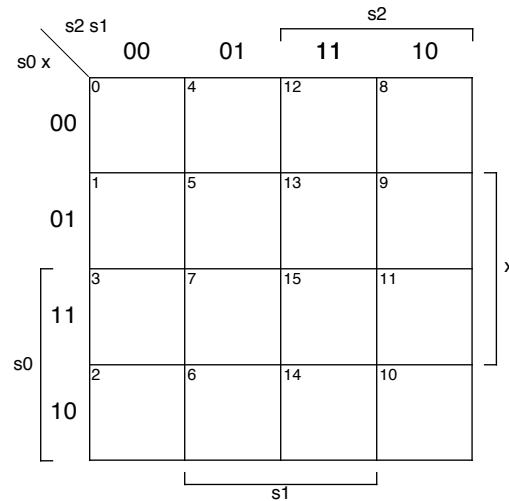
k2 =



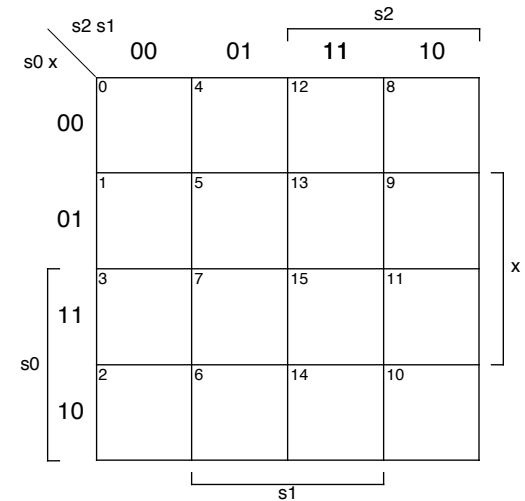
j1 =



k1 =



j0 =



k0 =

Next Time

- **Registers**
- **Memory**